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TECHNICAL INFORMATION

AUTOMATIC FREQUENCY CONVERTER

TYPE SA. 565

Operating and Maintenance Manual

Technical Handbooks Department

RACAL INSTRUMENTS LIMITED
Dukes Ride,
Crowthorne, Berkshire
England.

Tel: Crowthorne 5652

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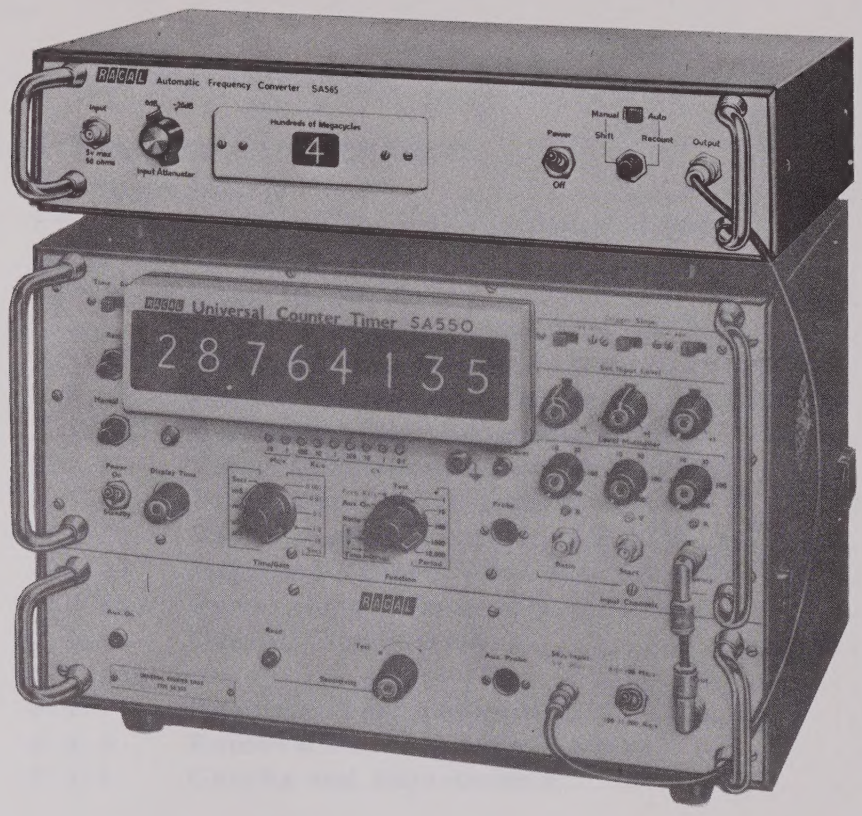

SA.565 AUTOMATIC FREQUENCY CONVERTER WITH SA.550 UNIVERSAL COUNTER-TIMER

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Ref. No.	Description
19-0001	Frequency Multiplier Assembly - Layout and Circuit
19-0002	Harmonic Generator Assembly - Layout and Circuit
19-0003	Balanced Mixer Assembly - Layout and Circuit
19-0004	Video Amplifier Assembly - Layout and Circuit
19-0005	Filter Detector Assembly - Layout and Circuit
19-0006	Shift Register Assembly - Layout and Circuit
19-0007	Sequence Control Assembly - Layout and Circuit
19-0061	Attenuator Assembly - Layout (for circuit see drawing ref. SA. 565).
19-0088	Rectifier Power Assembly - Layout (for circuit see drawing ref. 11-0033)

4. (Cont'd)

Ref. No.	Description
19-0090	Stabilizer Power Supply - Layout (for circuit see drawing ref. 11-0033)
19-0160	External Standard Assembly - Layout and Circuit
11-0033	Power Supply Assembly - Circuit
SA. 565	Detailed Interconnection Diagram

PART 1

TECHNICAL SPECIFICATION

1. TECHNICAL SPECIFICATION

1.1 Frequency Range	2 to 500 MHz
1.2 Input	
Sensitivity	0.1 to 1V r.m.s. on 0dB range, 1 to 5V r.m.s. on 20dB range.
Impedance	50 ohms.
Damage Overload	5V r.m.s. for both 0 and 20dB ranges.
Connection	BNC, front panel.
1.3 Output	
Frequency	2 to 102 MHz.
Amplitude	Greater than 100 mV r.m.s. into 50 ohms.
Connection	BNC, front panel
1.4 Frequency Standard - External	
Frequency	10 MHz
Amplitude	100mV to 10V r.m.s.
Input Impedance	Approximately 1 kilohm
Connection	BNC, rear panel
1.5 Accuracy	As external frequency standard
1.6 Measurement Time	0.5 seconds maximum.
1.7 Manual Operation	Push-button selection of heterodyne frequencies.
1.8 Ambient Temperature Range	0 to 45° C.

1.9 Power Input

Voltage	110, 120, 200, 220 or 240V r.m.s. ± 6%
Frequency	48 to 65 Hz
Power Consumption	25 watts
Connection	Rear panel socket
Fusing	AC power line and neutral, DC internal supplies.

1.10 Mechanical

Dimensions	Height:	3.5 in.	(9 cm.)
	Width:	16.75 in.	(42.5 cm.)
	Depth:	12 in.	(30.5 cm.)
Weight	10 lb. (4.5 kg.)		

1.11 Options

Auxiliary Output	Four-line BCD for 0, 1, 2, 3 or 4 hundreds-of-megahertz digit in 1248 code at nominal logic levels of 0V and + 6V

PART 2

OPERATION AND MAINTENANCE

2.1 OPERATING INSTRUCTIONS

2.1.1 PRELIMINARY CHECKS

2.1.2 Before operating the converter for the first time, the following points should be verified:

(1) That the POWER switch is OFF.

(2) That the voltage selector in the converter power unit is set in accordance with the available mains voltage.

(3) That the LINE and NEUTRAL mains supply fuses are rated in accordance with the available mains supply voltage.

Mains Voltage	Mains Fuse Ratings
200V, 220V, 240V	1 amp
110V, 120V	2 amp

2.1.3 The converter can now be connected to the mains and the power switched ON.

2.1.4 CHECKING THE COUNTER

2.1.5 The frequency measurement procedures given for the converter refer to its use in two different applications, namely,

(1) with the Racal Type SA.550,

(2) with any suitable non-Racal counter.

2.1.6 A procedure for checking the operation of the counter in application (1) will be found in the handbook for the Type SA.550. For details of how to check the counter in application (2), reference should be made to the appropriate manufacturer's handbook. Users are recommended to check the operation of the counter as a preliminary to carrying out any measurements.

2.1.7 OPERATING PROCEDURES

2.1.8 Though designed to be fully automatic in operation, the converter is also capable of being operated manually. This facility is of use (1) in test and maintenance generally, where it is advantageous to be able to set the local oscillator to a particular frequency and hold it there and (2) where the higher sensitivity obtainable in this mode makes it preferable to automatic working.

2.1.9 Connection of Converter OUTPUT Socket

2.1.10 Ensure that the OUTPUT socket of the converter is connected to the frequency measurement input socket of the counter (in the SA.550 application this is the front panel socket marked '50Ω INPUT, 5V MAX').

2.1.11 Connection of Converter 10 MHz REF IN Socket

2.1.12 Ensure that the 10 MHz REF IN socket of the converter is connected to the STD 10 MHz OUT socket of the counter (SA.550 application only) or to an equivalent source.

2.1.13 AUTOMATIC FREQUENCY MEASUREMENT

2.1.14 Use with Racal Type SA.550

2.1.15 On the counter:

(1) Set the FUNCTION switch to AUX ON, at the same time checking that the AUX ON indicator lamp lights up.

(2) Check that the TIME/EVENTS switch is set to TIME.

(3) Set the frequency channel SET INPUT LEVEL and LEVEL MULTIPLIER controls fully anti-clockwise.

(4) Check that the two sockets marked 'FREQUENCY' and 'OUTPUT' are connected to each other via the coaxial cable link provided.

(5) Turn the SENSITIVITY control fully clockwise.

(6) Set the frequency range selector switch to 0.1 - 100 MHz.

On the converter:

(7) Check that the POWER/OFF switch is set to POWER.

(8) Set the AUTO/MAN switch to AUTO.

(9) Set the INPUT ATTENUATOR to 20 dB.

(10) Apply the signal frequency to be measured to the INPUT socket.

(11) Check the display. If either of the digits 0 to 4 lights up, complete the measurement in accordance with operations (14) to (17). If, however, the legend CHECK LEVEL is displayed, proceed as follows:

(12) Set the INPUT ATTENUATOR switch to 0 dB.

(13) Re-check the display. If the legend CHECK LEVEL continues to be displayed, the input signal level is probably less than 100 mV (the sensitivity rating) and thus too low for the converter to operate.

(14) If there is sufficient signal level, the 'hundreds' digit will now be displayed. Operation of the SHIFT/RECOUNT button allows the system to recycle and may be used for checking purposes.

On the counter:

(15) Set the TIME/GATE switch as required.

(16) Set the DISPLAY TIME control as required.

On the two instruments:

(17) Read off the frequency of the input signal by adding the display on the converter (hundreds of megahertz) to the display on the counter (megahertz).

2.1.16 Use with Suitable Non-Racal Counters

2.1.17 No detailed procedures can be given here for using the SA.565 with suitable counters not manufactured by Racal. There is no difference in the manner in which the converter is used in such cases, but reference should be made to the appropriate manufacturer's handbook for details of how to use the counter.

2.1.18 MANUAL FREQUENCY MEASUREMENT

2.1.19 The procedure here is the same as that for automatic measurement except that it is carried out with the AUTO/MAN switch at MAN; in this position of the mode selector switch the SHIFT/RECOUNT push-button switch is used to perform the local oscillator frequency selection normally carried out by the automatic control system.

2.1.20 To illustrate the use of the SHIFT/RECOUNT push-button in manual frequency measurement, assume that the frequency of the input signal is in the range 202 MHz to 302 MHz. Whatever the actual signal frequency in this range, it can be shown that there are always two possible lower sideband responses, viz: the correct one due to the local oscillator frequency immediately below the signal (2) an ambiguous and incorrect response due to the local oscillator frequency setting immediately above the signal frequency.

In the case of a signal in the range 202 MHz to 302 MHz, the correct lower sideband response is obtained with the local oscillator frequency set to 200 MHz. This is the condition when digit '2' is displayed on the converter indicator panel, hence in the example chosen the SHIFT/RECOUNT push-button is operated as necessary until this particular digit is displayed.

2.1.21 Selecting the correct lower sideband response is equally straightforward for signal frequencies in either of the three ranges (1) 3 MHz to 102 MHz, (2) 302 MHz to 402 MHz and (3) 402 MHz to 502 MHz. Whereas in the case of signals in the range of 202 MHz to 302 MHz the SHIFT/RECOUNT is operated as required to bring up the digit '2', so in these three ranges it is operated as necessary to display '0', '3' and '4' respectively.

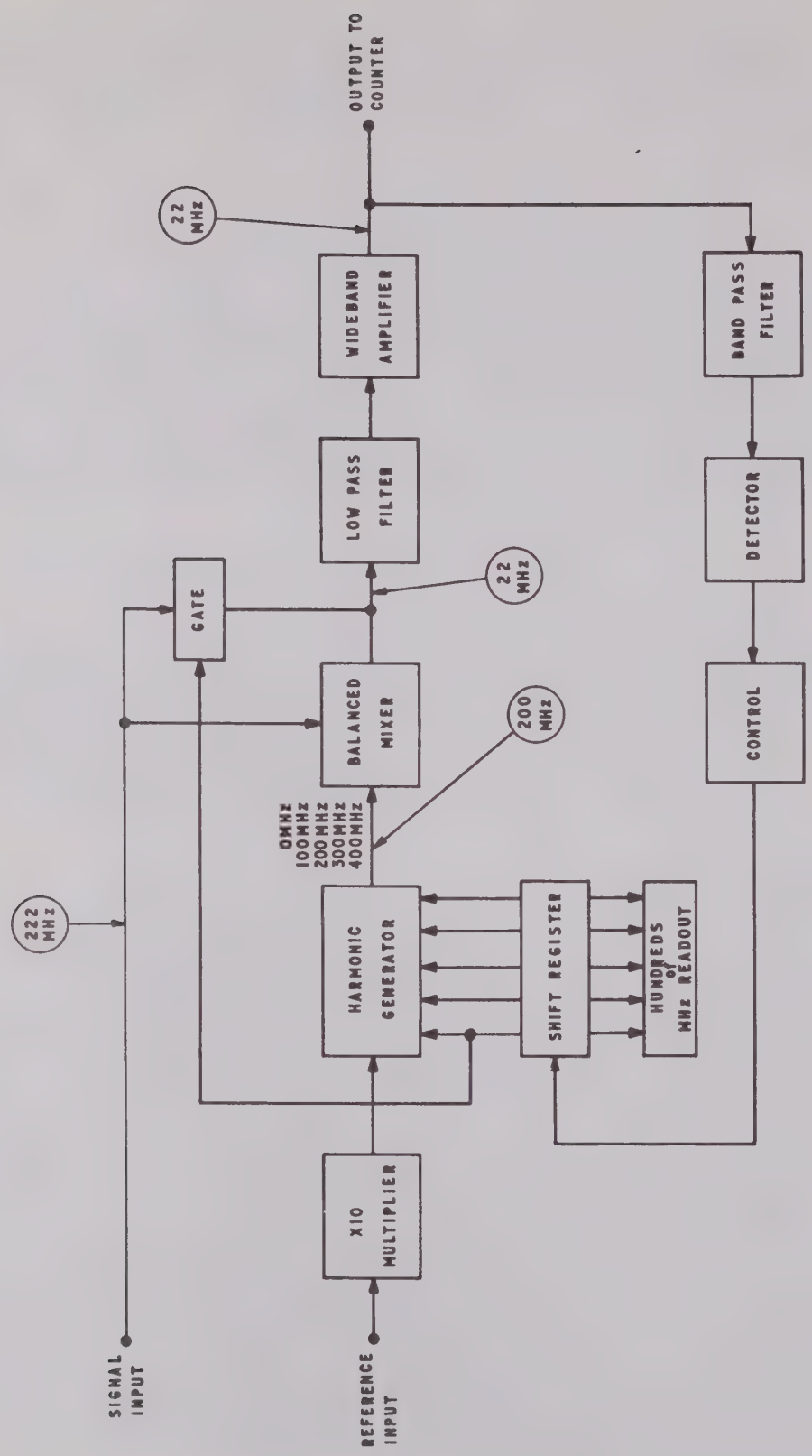
2.1.22 Manual selection of the correct lower sideband response for signals in the range 102 MHz to 202 MHz involves a slightly different approach since in the converter this range is covered in two stages, namely 102 MHz to 160 MHz and 160 MHz to 202 MHz. The point to note when measuring a signal in either of these frequency ranges is that the required 'hundreds of megahertz' (megacycles) display on the converter is the same in each case, i.e. digit '1'. To ensure selection of the correct range, the lowest range of all, viz: 3 MHz to 102 MHz, should be selected first (i.e. the SHIFT/RECOUNT button operated as required to bring up digit '0'). Having done this, the range 102 MHz to 160 MHz is selected by depressing the SHIFT/RECOUNT button once and range 160 MHz to 202 MHz by depressing it twice.

2.2 PRINCIPLES OF OPERATION (Fig. 2.1)

2.2.1 GENERAL

2.2.2 The reference frequency input is used, as shown in Fig. 2.1, to produce heterodyne harmonics at 100, 200, 300 and 400 MHz. One of these harmonics is then selected by the shift register for application, together with the signal frequency input, to the balanced mixer. The difference frequency output of the mixer, i.e. the signal frequency minus the selected harmonic, is applied to a low-pass filter and a wideband amplifier with a combined bandwidth of 2-102 MHz. The amplifier provides two outputs, one for the counter and the other for the converter frequency control circuits.

2.2.3 Consider, for example, the measurement by the converter and its associated counter of an input signal at a frequency of 222 MHz. In the converter the requirement is for the shift register to select the heterodyne harmonic at 200 MHz, i.e. the one immediately below the signal frequency, thus generating a difference frequency output from the mixer of 22 MHz. The required heterodyne harmonic is not, however, the only one that can beat with this signal frequency to generate a difference frequency that is acceptable to the counter.



SA.565 : SIMPLIFIED BLOCK DIAGRAM

Fig. 2.1

If, for example, the shift register were to select the 300 MHz heterodyne harmonic, the difference frequency output of the mixer would then be 78 MHz. Instead of the anticipated frequency measurement reading of 222 MHz the combined displays would then show 378 MHz. This cannot in fact occur with this particular system, by virtue of the fact that the shift register is made to select the heterodyne outputs of the harmonic generator not once but twice. The first heterodyne output selection sequence, called the 'A' scan, is terminated by the shift register control circuits immediately the mixer is made to generate an output within the passband of the counter input circuits. With the ending of the 'A' scan, the output of the harmonic generator is set to 0 MHz in readiness for the start of the second heterodyne selection sequence, called the 'B' scan. On the 'B' scan the frequency control circuits, advancing in 100 MHz steps, select and lock-on to the first sideband signal generated which is acceptable to the counter. Any possibility of error due to wrong heterodyne frequency selection is therefore eliminated since the first sideband signal generated is the result of applying the required heterodyne frequency.

2.2.4 OPERATION IN THE RANGE 2-102 MHz

2.2.5 The heterodyne principle of operation of the converter does not apply to signal frequency inputs in the range 2-102 MHz. For input signals within this range the signal frequency input by-passes the mixer and is applied instead directly to the input of the filtering and wideband amplifier circuits. The mixer by-pass gate is opened up to the signal frequency input during the period that the frequency control circuits are at 0 MHz.

2.2.6 AUTOMATIC LEVEL CHECK

2.2.7 In the absence of an input signal, the converter successively tries heterodyne frequencies of 0, 100, 200, 300 and 400 MHz in an attempt to find a response. During this time the legend CHECK LEVEL is displayed on the front panel. If, when the input signal is applied, its frequency or its amplitude is not within the limits specified (see Part 1) the legend will continue to be displayed, indicating that the signal cannot be measured.

2.2.8 When the input signal is applied, then providing its frequency and amplitude are such that it can be measured, it will beat with one or other of the heterodyne frequencies on the 'A' scan to provide a difference frequency that is acceptable to the counter. This condition is immediately detected by the automatic frequency control system which then (a) increases the sensitivity (to provide additional operating margins) and (b) sets the system to the condition where the mixer is by-passed. The heterodyne frequency is then advanced in 100 MHz steps until a response is obtained. The heterodyne frequency remains fixed at whichever setting the response occurs until either (a) the input signal is removed, (b) its frequency moves out of band, or (c) its amplitude falls below that necessary for correct operation.

2.2.9 The CHECK LEVEL legend displayed during the 'A' scan of the heterodyne frequencies is replaced at the end of the 'B' scan by a numerical display indicating the hundreds-of-megahertz to be added to the reading displayed on the counter.

2.3 TECHNICAL DESCRIPTION

NOTE: Most of the circuits referred to in the following paragraphs are represented on the block diagram, Fig. 2.15, following Part 2.4 (Maintenance). Detailed diagrammatic coverage of the instrument is given through Part 4 of the manual, which consists mainly of circuit and layout diagrams arranged in accordance with their six-digit assembly reference numbers. Part 4 ends in an overall diagram giving useful servicing information such as interconnection details, location of controls etc.

2.3.1 EXTERNAL STANDARD ASSEMBLY 19-0160

2.3.2 This assembly consists simply of a two-stage limiting amplifier (Q1 and Q2) the purpose of which is to standardise the 10 MHz external standard reference frequency input prior to its application to the frequency multiplier assembly 19-0001.

2.3.3 FREQUENCY MULTIPLIER ASSEMBLY 19-0001

2.3.4 This assembly comprises two stages of frequency multiplication, X5 and X2, through which the 10 MHz reference frequency passes before being applied to the harmonic generator assembly 19-0002.

2.3.5 The 10 MHz reference frequency input is multiplied first in the X5 circuit comprising diode D1, inductor L2 and capacitor C6, then in the X2 circuit D2, L4, C12. To obtain the increased signal level necessary for the correct operation of these circuits, each multiplier is preceded by a conventional class-A r.f. amplifier tuned to the appropriate frequency. The 100 MHz output is provided at the required level by means of the 100 MHz tuned r.f. amplifiers Q3 and Q4. The 100 MHz is taken from a tapping on the inductive element of the output tuned circuit to provide the required impedance match.

2.3.6 In the X5 and X2 circuits the multiplicative function is obtained by exploiting the particular property of the type of diode used, namely, its ability to develop an output waveform with a very fast rise-time when biased to operate in a certain mode; the diode is in each case self-biased to operate in this mode by a resistor of appropriate value (e.g. R6). The required harmonic is extracted from the harmonic spectrum present in this output waveform by the passive-tuned circuit of the multiplier (i.e. 5th harmonic of 10 MHz from L2 and C6 and 2nd harmonic of 50 MHz from L4 and C12).

2.3.7 The connection of the -12V power supply required to operate this particular assembly is dependent on conditions in the shift register assembly 19-0006. The supply is established in states 1A, 1B, 2, 3 and 4 of assembly 19-0006 but not in state 0 (see Part 2.3.41).

2.3.8 HARMONIC GENERATOR ASSEMBLY 19-0002

2.3.9 The function of the harmonic generator assembly 19-0002 is to multiply the 100 MHz reference harmonic input by a factor of either 1, 2, 3 or 4, depending on the conditions existing at the four numbered control terminals of the assembly. The multiplier circuits and their associated 100 MHz amplifiers are similar to those used in the frequency multiplier assembly 19-0001. In assembly 19-0002, however, the r.f. amplifiers are also used to facilitate selection of the required output frequency.

2.3.10 The base of each transistor in this assembly is set to a level of the order of -3.3V by means of the potential divider R2, R3. The gain of Q1 at 100 MHz is stabilized by the feedback resistor in the emitter circuit, R4; this increases the input impedance of the stage and makes it less dependent on the parameters of the transistor. The emitter load for Q1 is provided by R4, which is by-passed by C2. The collector circuit is broadly tuned to 100 MHz by the ferrite-cored inductor L1 connected in parallel with capacitors C3 and C4; C3 is the effective tuning capacitance, while C4 is included to isolate the diode biasing resistor R6 from the collector of the transistor. Stages Q2, Q3 and Q4 are similar to Q1, but since it is not required to drive a multiplier circuit, Q4 has a slightly different collector circuit arrangement. The capacitance tuning arm of this circuit comprises capacitors C12 and C13, which form a potential divider. Resistor R14 across the smaller of these two capacitors (C12) provides a d.c. return for the switching diode D1.

2.3.11 In each harmonic generator stage, the 100 MHz amplifier circuit is operative when its associated control terminal (1, 2, 3 or 4), and thus the junction point of its emitter resistors, is left free to fall to the level set by the base biasing resistors R2 and R3 (the emitter current of the amplifier transistor under these conditions is of the order of 11.4 mA). Conversely, if its control terminal is held at 0V approximately, the circuit is inoperative, the base-emitter junction of the transistor being reverse-biased by about -3.5V. Consider the case where the existing states on the control lines 1 to 4 are such that Q1 is operative and Q2, Q3 and Q4 are inoperative. With the potential at the junction of R4 and R5 free to fall to about -4V (the level determined by R2 and R3) the potential at the junction of R21 and R22 becomes sufficiently negative (about -0.4V) to maintain diode D7 in a forward-biased condition. The 400 MHz signal present at the tapping on the secondary winding of the X4 multiplier transformer T3 is thus fed through D7 and C14 to the common output terminal. The base-emitter junctions of Q2, Q3 and Q4, meanwhile, are reverse-biased by about 3.5V, thus making the junctions at the cathodes of diodes D5, D3 and D1 slightly positive (+1.3V). Any residual outputs at 100 MHz,

200 MHz and 300 MHz from the collector of Q1 and the X2 and X3 multiplier transformers (although Q2, Q3 and Q4 are inoperative, signals at a very low level are fed through the base-collector capacitances of the transistors) are now further attenuated in D1, D3 and D5 thus ensuring optimum purity in the frequency selected.

2.3.12 BALANCED MIXER ASSEMBLY 19-0003

2.3.13 This assembly uses two diodes in a double-balanced mixer circuit to ensure that both the signal frequency and the reference harmonic frequency are suppressed at the output. To provide the necessary balanced drive to the mixer diodes D2 and D3, wideband unbalance-to-balance transformers T1 and T2 are used on both the signal and reference harmonic frequency inputs.

2.3.14 The input impedance is of the order of 50 ohms over the input frequency range 2 MHz to 500 MHz. The bias current in the mixer diodes is provided by resistors R8 to R12; RV1 is adjusted for maximum rejection of reference harmonic frequency in the mixer output.

2.3.15 The non-linearity of the mixer diodes results in an output containing products at frequencies corresponding to the sum and the difference of its signal and reference harmonic frequency inputs. These products are coupled through to the output terminal of the assembly via capacitors C3 and C4.

2.3.16 With input frequencies in the range 2 MHz to 102 MHz the d.c. level at pin 21 is changed from zero volts to a negative voltage, thereby cutting off diodes D2 and D3 and switching on D1. The input signal now passes through diode D1 and the attenuator R2 and R4 to the output.

2.3.17 VIDEO AMPLIFIER ASSEMBLY 19-0004

2.3.18 This assembly consists of a four-stage wideband amplifier (Q1-Q4). A filter on the amplifier input (L1, C1-C3) limits the overall bandwidth to 110 MHz.

2.3.19 Inductor L2 and capacitors C9, C10 and C12 form an auxiliary low-pass filter. The control voltage from the shift register assembly 19-0006 is applied to resistors R11 and R12. This voltage may be either 0V or -4V. With 0V, diode D1 conducts and diodes D2 and D3 are reverse-biased, thereby switching the filter out of circuit. When a voltage of -4V is applied, D1 is reverse-biased and D2 and D3 conduct, thus placing the filter in the signal path.

2.3.20 The first of the wideband amplifier stages, Q1, is typical of the amplifier circuit arrangement as a whole. The stage is frequency

compensated by means of the trimmer capacitor, C7, connected in series with resistor R2 across R4. The +12V supply for Q2 is decoupled from the other four stages by R6 and C5.

2.3.21 In the gate stage the junction of R31 and R32 in the emitter of Q5 is taken via terminal 5 to the sequence control assembly 19-0007. Terminal 5 can be at either 0V or -6V, depending upon whether or not a signal is present (0V corresponds to the no-signal condition). The -6V condition signifies that Q5 is conducting normally, the junction of R31 and R32 then being left free to take up the base potential of the transistor, as set by the potential divider R28 and R29; under these conditions the signal at the input terminal of the board is fed via Q5 and its associated low-pass filter to the output terminal OUTPUT 1. When terminal 5 is at 0V (no-signal condition) Q1 is turned 'off' and zero signal is fed to the low-pass filter and OUTPUT 1. Resistor R31 in the gate stage helps to stabilize the gain, particularly at low frequencies. C29 is the by-pass capacitor for the emitter load R32.

2.3.22 The auxiliary low-pass filter in the output of Q5 has a sharp cut-off at 102 MHz and provides additional protection from interference signals of 102 MHz and above. If this filter were not included, false readings might well appear on the counter when the input signal to the converter is something of this order, e.g. 105 MHz. Under these conditions, in addition to the wanted signal frequency output (5 MHz), the unwanted signal frequency component at 105 MHz superimposed on this would also be fed to the counter. As it is, the filter removes the 105 MHz component and passes the wanted 5 MHz signal through to the counter. The gate stage Q5 has a nominal voltage gain of 1 and so provides, in addition to the gating, buffering facilities for the filter.

2.3.23 FILTER, DETECTOR ASSEMBLY 19-0005

2.3.24 The signal frequency input to this assembly is fed to buffer Q1, the main low-pass filter, buffer Q2, the auxiliary high and low-pass filters and detector Q3 and Q4.

2.3.25 Resistor R1 in the input has a two-fold function: (1) it terminates the output of the video amplifier assembly 19-0004, (2) it provides a d.c. return path for the base current of Q1. Q1 is another grounded-emitter stage and is included to buffer the main low-pass filter from the input circuit and also from the auxiliary low-pass filter on the output of Q5. Resistor R3 in the emitter of Q2 is by-passed by C28 to provide high-frequency boost. The main emitter load resistor R4 is by-passed by C4.

2.3.26 The input end of the main low-pass filter contains the matching circuit C5, R5 and R6. The filter proper comprises L1-L4 and C6-C14, is m-derived, and has a very sharp cut-off at 102 MHz. The filter is terminated by R7, which also serves to provide a d.c. return path for the base current of Q2.

2.3.27 Q2 is a grounded-emitter stage similar to Q1 but with an emitter-peaking facility (C18). This stage buffers the auxiliary high and low-pass filters from the main low-pass filter.

2.3.28 Inductor L5 and capacitors C17, C19 and C20 form a simple high-pass filter in the output of Q2, L5 being adjusted so as to attenuate signal frequencies below 2 MHz. Signals above this frequency are passed by the filter through to the detector, Q3 and Q4. The base-emitter junction of Q3 detects the level of signal, the resulting d.c. being amplified in the collector circuit. Further d.c. amplification occurs in Q4.

2.3.29 The auxiliary high and low-pass filters across the input of the detector (L7 and C22; L9 and C25) are switched in and out of circuit by voltage levels from the shift register assembly 19-0006. The auxiliary high-pass filter is series resonant at approximately 20 MHz but its effect in the circuit is negligible except when the diode D1 is forward-biased (state 1B of the shift register assembly); under these conditions the reduced impedance of the diode allows current to pass through the filter, and any signals which are passed through the main filter and buffer Q2 are attenuated at 20 MHz. Similarly, the auxiliary low-pass filter, which is series resonant at about 90 MHz, is effective only when diode D2 is forward-biased (state 1A of the shift register assembly); in this case any signals passing through the main filter and buffer are attenuated at approximately 90 MHz before they are passed to the detector.

2.3.30 SHIFT REGISTER ASSEMBLY 19-0006

2.3.31 Inputs

2.3.32 The shift register assembly 19-0006 is designed to accept the following inputs:

(a) A reset pulse,

(b) shift pulses, and

(c) a carry level.

2.3.33 Reset Pulse Input This input originates in the main reset generator circuit of the sequence control assembly 19-0007. The 21V nominal peak-to-peak pulse (approximate upper and lower limits +12V and -9V respectively) is d.c. coupled (1) via resistor R10 to the base of the right-hand transistor of flip-flop 0 (Q3) and (2) via resistors R13, R22 etc., to the bases of the left-hand transistors in all the other flip-flops (Q6, Q10 etc.). The negative-going edge of the pulse turns all these transistors 'on', thereby causing the register to take up the condition known as state zero (0). The states of the individual transistors following a reset pulse are shown in Table 2.1. *

2.3.34 Shift Pulses Input This consists of the output of the sequencing generator circuit in assembly 19-0007 differentiated by capacitor

* See page 15

C5 on that assembly and resistors R50 and R51 in the shift register assembly. The line on which the differentiated positive and negative going shift pulses appear is coupled via diodes D4, D8 etc., to the bases of the right-hand transistors of all of the flip-flops (Q3, Q8 etc.). Whenever any one of these transistors is conducting, its base, and therefore the cathode of the associated diode, is slightly negative. When the positive-going shift input pulse exceeds the reverse bias on the diode (the diode anodes all receive a standing bias of -6V from the junction of resistors R50 and R51) the diode conducts and the transistor is turned 'off'.

2.3.35 Carry Level Input This consists of the positive-going level change at Q18 collector when this transistor is turned 'on', fed back to the input of the register via an external linkage on the interconnecting assembly 19-0008. From the point at which it is fed back into the shift register again (terminal 1) the carry level is coupled, via a differentiating circuit and a steering diode (C1, R2 and D1) to the base of transistor Q1 in flip-flop 0. When this transistor is conducting, the d.c. levels at its base and its collector are such that the steering diode is biased in a forward direction. Consequently, if a carry level is present, this will be fed through the steering diode to Q1 base, thus causing the transistor to be turned 'off'.

2.3.36 Circuit Operation

2.3.37 Assume that the shift register has been reset to state zero as described in paragraph 2.3.33. The first positive-going shift pulse to occur following a reset action turns transistor Q3 of flip-flop 0 'off'; all the other transistors to which the shift input is applied are 'off' already, hence flip-flop 0 is the only circuit affected by this particular shift pulse. Since Q3 of flip-flop 0 has been turned 'off', Q1 in this circuit must now be conducting. As transistor Q1 comes 'on', a positive-going edge similar to the carry level input appears at Q1 collector, which, again like the carry level input, is a.c. coupled via a differentiating circuit and a steering diode (C2, R14 and D5) to the base of the following transistor, Q6. Since Q6 is conducting, the steering diode D5 is forward-biased, consequently the positive-going edge at the collector of Q1 passes through the diode to Q6 base thus causing Q6 to be turned 'off'. The register has now changed from its initial zero state condition to the condition known as state 1A.

2.3.38 The second shift input pulse to occur after a reset action has taken place changes the state of flip-flops 1A and 1B in exactly the same way as the first shift input pulse changed the states of flip-flops 0 and 1A. This type of action continues with the third, fourth and fifth shift input pulses, which change the states of flip-flops 1B and 2, 2 and 3, and 3 and 4 respectively. Conditions at the end of the fifth shift input pulse are such that when the sixth pulse occurs, the effect on the register is the same as that of applying a reset pulse, i.e. the register is returned to the state from which it started, namely, state zero.

2.3.39 Control Functions

2.3.40 The changes of state in the various flip-flop circuits as the register runs through a complete cycle is used to bring about changes in the instrument operating conditions as follows.

2.3.41 Flip-flop 0 Assume this circuit to be in the second of its stable states, i.e. the state Q1 fully 'on', Q3 fully 'off'. In order to get the circuit to change back to its initial stable state, transistor Q1 must receive a carry level input from flip-flop 4 (via the linkage on assembly 19-0008) or, alternatively, transistor Q3 must receive a reset pulse from the main reset generator circuit in the sequence control assembly 19-0007. As soon as either of these two inputs is received, current starts to flow out of Q3 emitter into the base-emitter junction of transistor Q2. When Q3 is fully 'on' Q2 'bottoms' thus causing the voltage at Q2 collector to fall to zero. The collector of Q2, however, is coupled (1) via diode D2 to the '0' bulb in the display assembly 23-1005 and (2) via emitter-follower Q4 to the -12V power supply input terminal on the frequency multiplier assembly 19-0001. Consequently, the result of Q2 'bottoming' is, first, that current flows out of the register, through D2 to the '0' bulb thus turning this 'on' and, secondly, that the voltage at the -12V power supply input terminal of the frequency multiplier assembly falls to zero, thereby making this assembly inoperative.

2.3.42 As flip-flop 0 changes back to its initial stable state, the change in transistor Q3 is accompanied by a similar but opposite change in the condition of transistor Q1. The diminishing current in Q1 collector circuit makes the voltage at the junction of resistors R3 and R4 increase until, eventually, when Q1 is turned fully 'off', it reaches approximately -4V. Now the collector of Q1 is also connected, via resistor R6, to pin 21 in the balanced mixer assembly 19-0003. As Q1 goes 'off' the -4V level which appears on its collector cuts off diodes D1 and D2 in the mixer assembly and switches on diode D1. In the mixer, therefore, the input signal now passes through diode D1 and the attenuator R2 and R4 to the output.

2.3.43 The '0' bulb has a common connection with all the other digit bulbs in the display assembly. This common connection is taken to the emitter of emitter-follower Q14 in the control flip-flop circuit of

the sequence control assembly. Depending on the state of the control flip-flop the voltage level at Q14 emitter is either 0V (control flip-flop reset, digit display 'off') or -12V (control flip-flop triggered, digit display 'on'). When the 0V level is present, diode D2 in the shift register prevents Q3 collector from taking up a similar level, which in turn prevents spurious cut-offs in the -12V power supply to the frequency multiplier assembly.

2.3.44 Flip-flops 1A and 1B These complementary flip-flops are basically the same circuit as the 0 flip-flop. This being the case, when they are triggered, the collector voltages on their left-hand transistors (Q6 and Q10) increase to about -4V as these are turned 'off', whilst the currents in the emitters of their right-hand transistors (Q8 and Q11) increase to a maximum as these go fully 'on'.

2.3.45 In the 1A flip-flop, the appearance of the -4V edge at Q6 collector has two main effects, namely, (1) it turns 'on', via the 'or' gate diode D6, the 100 MHz circuit in the harmonic generator assembly and (2) it switches into circuit, via emitter-follower Q5, the low-pass auxiliary filters in the video amplifier and filter detector assemblies. The corresponding event in the 1B flip-flop has similar effects, i.e. (1) it turns 'on' the 100 MHz circuit in the harmonic generator assembly via the other half of the 'or' gate, diode D10, and (2) switches into circuit, via emitter-follower Q9, the high-pass auxiliary filter in the filter detector assembly. The increased currents flowing in the emitters of transistors Q8 and Q9 when these are turned 'on' have the same effect externally, i.e. they turn 'on', via transistor Q7, the '1' digit bulb in the display indicator assembly.

2.3.46 Flip-flops 2, 3 and 4 The collector load resistors of transistors Q12, Q15 and Q18 of flip-flops 2, 3 and 4 are connected up to the emitter circuits of the 200 MHz, 300 MHz and 400 MHz selector stages of the harmonic generator assembly, where they provide the bias necessary to turn these stages 'on' and 'off' as required. The three right-hand transistors of these flip-flops have their emitters coupled, via identical drive stages (Q13, Q16 and Q19) to the '2', '3' and '4' digit bulbs respectively in the display indicator assembly.

2.3.47 With their collector load resistors connected, flip-flops 2, 3 and 4 are identical to flip-flops 0, 1A and 1B. The -4V edge which occurs at the collectors of the left-hand transistors when the flip-flops are triggered turns the 200 MHz, 300 MHz and 400 MHz circuits in the harmonic generator assembly 'on'. The current drive from the emitters of the right-hand transistors into the bases of Q13, Q16 and Q19 turns the '2', '3' and '4' digit bulbs 'on'.

TABLE 2.1

FLIP-FLOP	TRANSISTORS	0	1A	1B	2	3	4	0
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)
0	Q1	−	+	+	+	+	+	−
	Q3	+	−	−	−	−	−	+
1A	Q6	+	−	+	+	+	+	+
	Q8	−	+	−	−	−	−	−
1B	Q10	+	+	−	+	+	+	+
	Q11	−	−	+	−	−	−	−
2	Q12	+	+	+	−	+	+	+
	Q14	−	−	−	+	−	−	−
3	Q15	+	+	+	+	−	+	+
	Q17	−	−	−	−	+	−	−
4	Q18	+	+	+	+	+	−	+
	Q20	−	−	−	−	−	+	−

NOTE:- In the above table the plus signs indicate the transistors which are conducting and the minus signs those which are non-conducting.

2.3.48 SEQUENCE CONTROL ASSEMBLY 19-0007 (Fig. 2.2) *

2.3.49 Circuit Breakdown

2.3.50 The sequence control assembly 19-0007 contains the following circuits:-

(a) Input trigger.

* See page 21

(b) Sequencing generator.
(c) And-gate.
(d) Delay generator.
(e) Control flip-flop.
(f) Auxiliary reset generators.
(g) Main reset generator.

2.3.51 Input Trigger

2.3.52 The input trigger circuit comprises an emitter-follower (Q1), a Schmitt trigger (Q1, Q2) and a trigger level (sensitivity) control stage (Q4).

2.3.53 The base of the emitter-follower, Q1, is coupled directly to the output of the detector circuit in the filter detector assembly. Resistor R12 in the trigger level control circuit is connected to the junction of resistors R32 and R33 in the collector (output) circuit of transistor Q10 of the control flip-flop.

2.3.54 Under 'A' scan conditions, first, the input level to Q1 base is zero volts, secondly, Q10 in the control flip-flop is turned fully 'on'. In the Schmitt trigger circuit, in its quiescent state, the left-hand transistor, Q2, is 'on' (Q5 base slightly positive) and the right-hand transistor, Q3, 'off'. In the trigger level control circuit, the level at the emitter of Q4 is of the order of +2V (set by potentiometer RV1).

2.3.55 Prior to the transition from 'A' to 'B' scan conditions, the output of the detector increases in proportion to the level of the signal it receives from the r.f. circuits preceding it. When this output level reaches +1.5V, Q2 in the Schmitt trigger circuit is made to cut-off and the circuit changes over to the state Q2 'off', Q3 'on'. Following the start of the 'B' scan, conditions in the r.f. circuits of the instrument are such that the detector output once again falls to zero. When the falling detector output reaches the lower trigger level of the Schmitt, the trigger circuit is forced back to its original condition, i.e. Q2 'on', Q3 'off'.

2.3.56 Approximately 3 mS after the start of the 'B' scan, the delay generator reverts to its stable state and the resulting circuit output triggers the control flip-flop, which thus takes up the state Q10 'off', Q12 'on'. As Q10 goes 'off' it alters the level at the emitter of Q4 in the trigger level control circuit to approximately 1.25V (this level is set by potentiometer RV2).

2.3.57 Prior to the end of the 'B' scan, the output of the detector once more increases in proportion to the level of the signal fed to it from the video amplifier assembly. When the detector output reaches +0.95V,

transistor Q2 in the Schmitt trigger circuit is forced 'off' again and the circuit becomes stable with Q2 cut-off and Q3 conducting. The Schmitt remains in this condition until such time as there is a change in the frequency or the amplitude of the signal at the input of the detector sufficient to cause the detector output level to fall below the second lower threshold level of the input trigger circuit. When this happens, the Schmitt trigger is forced back to its original stable state ('A' scan conditions again) and the control flip-flop is reset. With the control flip-flop reset, Q10 in this circuit comes back 'on' again and the emitter of Q4 in the trigger level control circuit returns to its original level (+2V approximately). Consequently, when the input trigger circuit does operate again it does so at the higher of its two trigger level settings, i.e. at +1.5V instead of +0.95V.

2.3.58 Circuit Outputs The input trigger circuit provides two outputs, one feeding the sequencing generator gate and the other feeding the auxiliary reset generator 'A'; both outputs come from the collector of Q3. The direct effects of these outputs are described in the paragraphs dealing with the circuits concerned.

2.3.59 Sequencing Generator

2.3.60 The sequencing generator comprises an astable flip-flop (Q6, Q7) and a transistor gate (Q5).

2.3.61 Circuit Operation The base of the gate transistor, Q5, is coupled, via the potential divider R10, R13, to the output of the Schmitt section of the input trigger circuit (Q3 collector). Under 'A' scan conditions, the trigger circuit output level fed to the potential divider on Q5 base is approximately -9V, the gate is open (Q5 base-emitter junction forward-biased) and the flip-flop free-runs. At the end of the 'A' scan, when the input trigger circuit is operated, the level at Q3 collector rises to about +1V, the sequencing generator gate closes (Q5 base emitter junction reverse-biased) and the flip-flop stops. Shortly after it is operated, the input trigger circuit is forced back to its original condition, the sequencing generator gate re-opens and the flip-flop starts up again. At the end of the 'B' scan, when the input trigger circuit is re-operated, the sequencing generator gate closes again and the flip-flop stops. The sequencing generator circuit remains in this condition until such time as there is a change in the amplitude or frequency of the signal fed to the filter detector assembly sufficient to cause the input trigger circuit to operate again. When this happens, the trigger circuit reverts to its 'A' scan condition and the circuit action just described is repeated.

2.3.62 External Outputs The edge developed at the collector of Q5 as this transistor changes state is used to control the state of the gated output buffer stage, Q5, in the video amplifier assembly. When Q5 in this assembly is conducting, Q5 in the video amplifier assembly is non-conducting, and vice-versa.

2.3.63 The 35 mS pulses developed at the collector of Q7 when the sequencing generator flip-flop is free-running are used to drive the shift register assembly. The drive pulses are applied to the shift register via a simple differentiating circuit, viz: C5 in the sequence control assembly combined with R50 and R51 in the shift register assembly.

2.3.64 Internal Output The sequencing generator circuit provides one internal output, namely, that to the And-gate circuit from the collector of transistor gate, Q5. The direct effect of this output is decsribed in the following paragraphs.

2.3.65 And-gate

2.3.66 The And-gate circuit comprises just two diodes (D2 and D3) and a resistor (R21).

2.3.67 Circuit Operation The anode of diode D2 is coupled directly to the collector of the sequencing generator gate transistor, Q5. The anode of diode D3 is coupled directly to the collector of the right-hand transistor, Q12, of the control flip-flop. Under 'A' scan conditions Q5 and Q12 hold the anodes of D2 and D3 at potentials of 0V and -10V respectively. Since D2 is forward-biased, the output of the gate is negligible.

2.3.68 At the end of the 'A' scan, when the voltage at Q12 collector is still at -10V, Q5 collector falls to -6V, taking the output of the and-gate with it. Shortly after it falls to -6V, the level at Q5 collector returns to 0V, restoring the forward-bias on diode D2, thus causing the and-gate output to become negligible again. When the control flip-flop resets later on in the 'B' scan, Q12 collector goes to 0V, diode Q3 becomes forward-biased thus causing the gate to be inhibited. At the end of the 'B' scan, Q5 collector returns to its -6V level, but since the level at Q12 collector is still 0V, the and-gate remains inoperative. The and-gate remains in this condition until such time as there is a change in the frequency or the amplitude of the signal fed to the filter detector assembly sufficient to cause the control flip-flop to be reset. When this happens, Q12 collector returns to its original level (-10V) and the circuit action just described is repeated.

2.3.69 Circuit Output The and-gate output is fed directly to the input of the delay generator circuit, where its effect is as described in the following paragraphs.

2.3.70 Delay Generator

2.3.71 Together with their associated components, the delay generator transistors Q8 and Q9 form a monostable flip-flop.

2.3.72 Circuit Operation The base of the left-hand transistor, Q8, of the delay generator flip-flop, is coupled, via diode D4 and the differentiating circuit C6, R22, to the output of the and-gate circuit. Under 'A' scan conditions the and-gate output is at a fixed potential of approximately -0.5V. In the delay generator flip-flop, in its quiescent state, (1) transistor Q9 is held 'on' by the current fed into its base via resistor R28, and (2) transistor Q8 is held 'off' by the small positive bias applied to its base-emitter junction from the potential divider R23, R25 and R27.

2.3.73 When the and-gate operates at the end of the 'A' scan, the level fed to the input of the delay generator flip-flop falls sharply towards -6V. This negative-going edge is differentiated by C6, R22 and then fed, via diode D4 to the base of transistor Q8. This transistor is thus made to conduct, thereby causing the flip-flop to take up its quasi-stable state, namely, Q8 'on', Q9 'off'. Capacitor C8, once it is fully charged, discharges through resistor R28, until, after 3 mS approximately, the flip-flop reverts to its original (stable) condition. The circuit will remain in this condition until such time as there is a change in the amplitude or the frequency of the signal fed to the filter detector assembly sufficient to result in the resetting of the control flip-flop. When this happens, the and-gate will operate again at the end of the next 'A' scan and the circuit operation just described will be repeated.

2.3.74 Circuit Outputs The delay generator circuit provides two outputs, namely, (1) the output to the control flip-flop from the collector of transistor Q8, and (2) that to the main reset generator circuit from the collector of transistor Q9. The direct effects of these two outputs are described in the paragraphs immediately following and in those dealing with the main reset generator circuit.

2.3.75 Control Flip-flop

2.3.76 Basically, this is just a straightforward bistable flip-flop (Q10, Q12) equipped with differentiating input circuits and steering gates (C9, R30, D5 and C12, R38, D7). The two other stages associated with the control flip-flop (Q11 and Q13, Q14) are concerned with the operation of the display indicator assembly and are dealt with separately in para. 2.3.79.

2.3.77 Circuit Operation The base of transistor Q10 of the control flip-flop is coupled (1) via resistor R29 to the output of the main reset generator and (2) via steering diode D5 and differentiating circuit C9, R30, to the output of the delay generator. At the start of the 'A' scan, the main reset generator is triggered. The resulting reset pulse is fed, via R29, to the base of Q10, where the negative-going edge of the pulse turns the transistor 'on'. The control flip-flop is thus now in the stable state Q10 'on', Q12 'off'. On the changeover from 'A' to 'B' scan conditions, the main reset generator circuit is triggered again, but this time the reset pulse has no effect on the control flip-flop as this has not left its reset condition. Later on in the 'B' scan, when the

delay generator reverts to its original (stable) state, the resulting positive-going edge, differentiated by C9 and R30 and subsequently fed via diode D5 to Q10 base, turns this transistor 'off'. The control flip-flop stays in the condition Q10 'off', Q12 'on' until such time as there is a change in the amplitude or the frequency of the signal fed to the filter detector assembly sufficient to result in the main reset generator circuit being re-triggered. When this happens, the resulting reset pulse returns the control flip-flop to its original (reset) condition as already described, subsequent to which the circuit is triggered again at the appropriate point in the 'B' scan, by the output of the delay generator.

2.3.78 Circuit Outputs The control flip-flop provides five outputs, three from the left-hand transistor, Q10, and two from the right-hand transistor, Q12. The outputs from Q10 consist of (1) the collector circuit output to the input trigger circuit, (2) the collector circuit output to diode D8 and the auxiliary reset generator 'A' circuit and (3) the emitter circuit output to the base of transistor Q11. The outputs from Q12 comprise (1) the output to the and-gate and (2) the output fed via resistor R41 to the base of transistor Q13. The effect of the outputs fed to the input trigger and and-gate circuits has been described already in the sections dealing with these particular circuits. The effect of the outputs to transistors Q11 and Q14 is dealt with in the paragraphs immediately following and that of the output to auxiliary reset generator 'A' in para. 2.3.82.

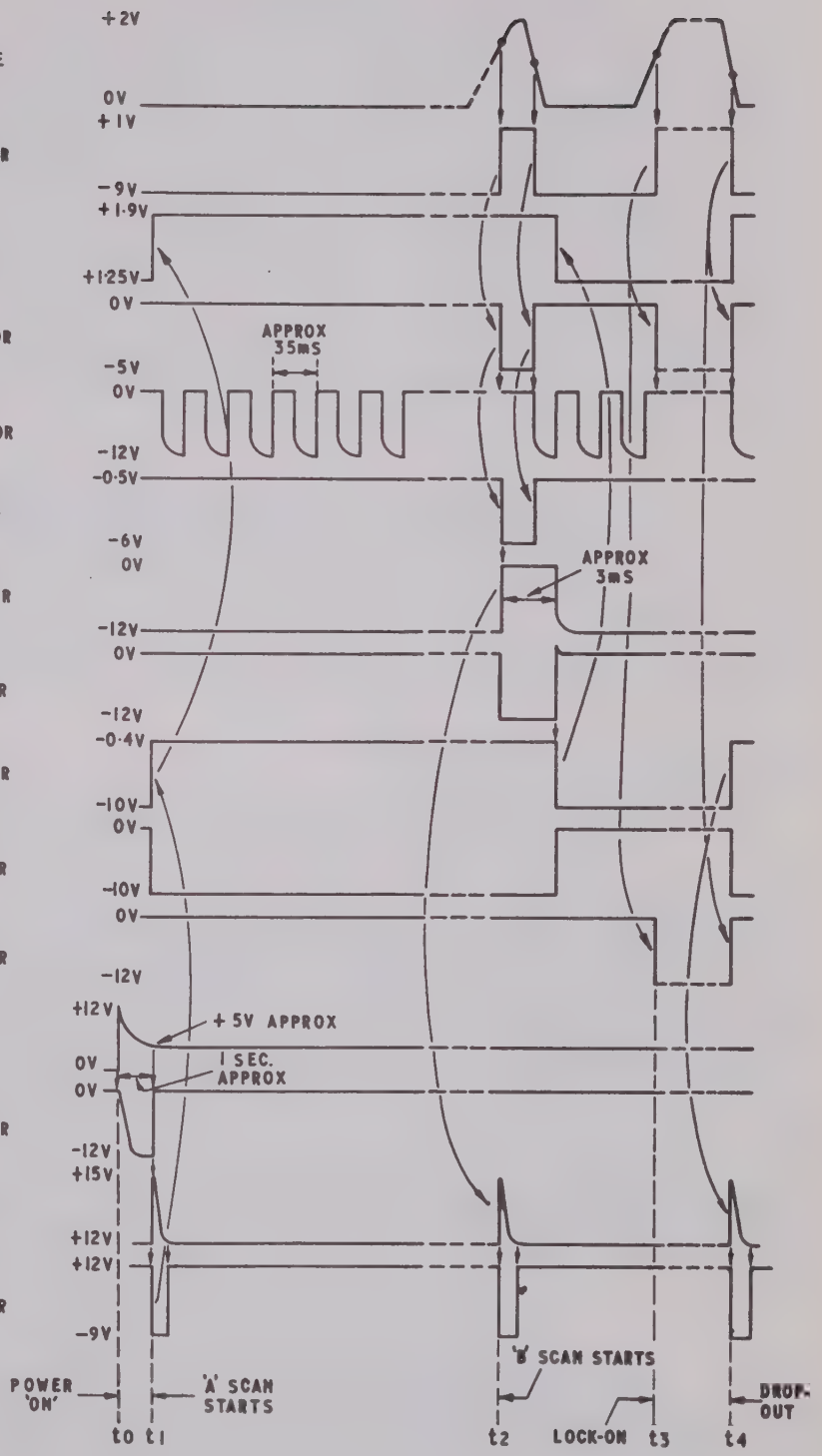
2.3.79 Transistors Q11, Q13 and Q14 are concerned with the operation of the display indicator assembly. Resistor R36 in the collector circuit of Q11 is connected to one end of the 'check level' lamp, its other end being connected to -12V in the display assembly. The emitter of transistor Q14 is connected to the common line terminals of the digit lamps in the display assembly, the other sides of the lamps being connected to the collectors of the digit bulb drive transistors in the shift register assembly. Under 'A' scan conditions, when transistor Q10 of the control flip-flop is 'on', transistor Q11 is also 'on' and this supplies the necessary current to operate the 'check level' lamp. The collector voltage of the 'off' transistor (Q12) holds the grounded-emitter stage Q13 'on', with the result that both base and emitter of the emitter-follower Q14 are at a potential of the order of 0V, and the digit display is thus 'off'. Conversely, when the left-hand transistor of the flip-flop, Q10, is turned 'off' ('B' scan conditions), Q11 is turned 'off' thus making the 'check level' display inoperative, and (2) Q13 is turned 'off', thus causing the collector to fall to -12V, which fall is then transferred by the emitter-follower action of Q14 to reactivate the digit display.

2.3.80 Auxiliary Reset Generators

2.3.81 There are two auxiliary reset generator circuits, viz:-

(a) Auxiliary reset generator 'A'
(b) Auxiliary reset generator 'B'

WAVEFORM REF.	CIRCUIT	LOCATION IN CIRCUIT
A	INPUT TRIGGER	Q1 BASE
B	INPUT TRIGGER	Q3 COLLECTOR
C	INPUT TRIGGER	Q4 EMITTER
D	SEQUENCING GENERATOR	Q5 COLLECTOR
E	SEQUENCING GENERATOR	Q7 COLLECTOR
F	AND-GATE	D2 CATHODE
G	DELAY GENERATOR	Q8 COLLECTOR
H	DELAY GENERATOR	Q9 COLLECTOR
J	CONTROL FLIP-FLOP	Q10 COLLECTOR
K	CONTROL FLIP-FLOP	Q12 COLLECTOR
L	AUX. RESET GENERATOR 'A'	Q15 COLLECTOR
M	AUX. RESET GENERATOR 'B'	Q16 BASE
N	AUX. RESET GENERATOR 'B'	Q16 COLLECTOR
O	MAIN RESET GENERATOR	Q17 BASE
P	MAIN RESET GENERATOR	Q17 COLLECTOR



NOTE :- CAUSE–EFFECT RELATIONSHIP BETWEEN WAVEFORMS SHOWN BY LINK-UP ARROWS

Fig. 2.2

2.3.82 Auxiliary Reset Generator 'A' The base of transistor Q15 is coupled via resistor R45 to the output of the input trigger circuit (Q3 collector). The collector of Q15 is coupled via diode D8 to the collector of transistor Q10 in the control flip-flop. Under 'A' scan conditions the level at Q3 collector in the input trigger circuit is about -9V, whilst the level fed to Q15 collector via D8 is approximately 0V. At the end of the 'A' scan the first-named level goes to +1V approximately, but as Q15 collector is still held at 0V by the control flip-flop output, there is no change at this point. Later on in the 'B' scan the control flip-flop is triggered and the output at Q10 collector falls to -10V. At the end of the 'B' scan the output of the input trigger circuit goes sharply positive to approximately +1V. As the inhibit level applied to the collector of Q15 has now been removed, the positive-going edge from the input trigger circuit is inverted and appears at Q15 collector as a 12V negative-going edge.

2.3.83 Auxiliary Reset Generator 'B' The base of transistor Q16 is fed from the time constant circuit C13, R47. When the instrument is first switched on C13 charges up and holds Q16 'off' for the time (one second approximately) Q16 base takes to fall from +12V to approximately +5V. When the base potential of Q16 reaches +5V, the transistor comes 'on' and a positive-going 12V edge is developed at its collector.

2.3.84 Main Reset Generator

2.3.85 The base of the main reset generator transistor, Q17, is connected (1) via resistor R53 to the -12V supply and (2) via the three coupling circuits R49, C16, R50, C17 and R48, C15 to the outputs of the delay generator and both auxiliary reset generators. The operation of the main reset circuit is the same for all three inputs, i.e. the positive-going edge of the incoming pulse turns the transistor 'off' (normally it is held 'on' by the current flowing into its base via resistor R53) thus causing its collector to fall sharply negative from +12V to approximately -9V. When the circuit has recovered through R53, the transistor comes back 'on' again, thus causing the voltage at the collector to return again to its original level, namely, +12V.

2.3.86 POWER SUPPLY ASSEMBLY 11-0033

2.3.87 This assembly provides the +12V and -12V power supplies used by the majority of the circuits in this instrument.

2.3.88 +12V Power Supply The unstabilized d.c. power supply to the +12V stabilizer circuit is derived from the full-wave rectifier diodes D5 to D8, capacitor C2 and resistor R1. Overload protection for the mains transformer and the rectifier diodes is provided by fuse F3.

2.3.89 Transistor Q1 is the series stabilizer for the +12V supply. The conduction of Q1 is controlled by the current through transistor

Q2, which in turn depends on the current output of an error-sensing stage (Q6) and its associated constant-current source (Q5, D15, R9, R11). Changes in the output voltage on the +12V line are detected via the resistive chain R15, RV1, R17. This produces a change in the current fed into the base of Q6 and, consequently, a change in the current through Q6 collector. However, as the collector of Q6 is fed from a constant-current source, any change of current in the Q6 collector must result in an equal and opposite change of current into the base of Q2. After amplification in Q2, the current change is further amplified in the series stabilizer Q1. The final current change in Q1 emitter is of the correct phase and amplitude to restore the +12V output to its right value.

2.3.90 To minimize changes in Q6 base potential, Zener diode D13 is chosen to counter-balance the change in Q6 base-emitter voltage with temperature.

2.3.91 -12V Power Supply The details and operation of the -12V power supply circuit are exactly the same as for the +12V circuit except that its constant-current source is provided by the +12V supply and resistor R10.

2.3.92 OVERALL DESCRIPTION

2.3.93 R.F. Circuits

2.3.94 General The general operation of the r.f. circuits of the instrument is adequately covered in Part 2.3 of the handbook.

2.3.95 Suppression of Unwanted Responses In Part 2.3, only the required output of the balanced mixer, namely the signal frequency (fs) minus the selected heterodyne harmonic (fo), has been considered. In addition to this output ($f_s - f_o$) various other outputs do, of course, exist and these can be of significance whenever f_s and f_o are near to or within the i.f. bandwidth of the signal circuits.

2.3.96 Consider for example the case where f_s is equal to 104 MHz and f_o is equal to 100 MHz. Discounting the required output of the balanced mixer ($f_s - f_o$) other significant outputs are present as follows:-

(1)	(2)	(3)	(4)	(5)	(6)
f_s	f_o	$f_o + f_s$	$2f_s$	$2f_o$	2nd and 3rd order sum and difference
104	100	204	208	200	frequencies

NOTE: All frequencies are in MHz.

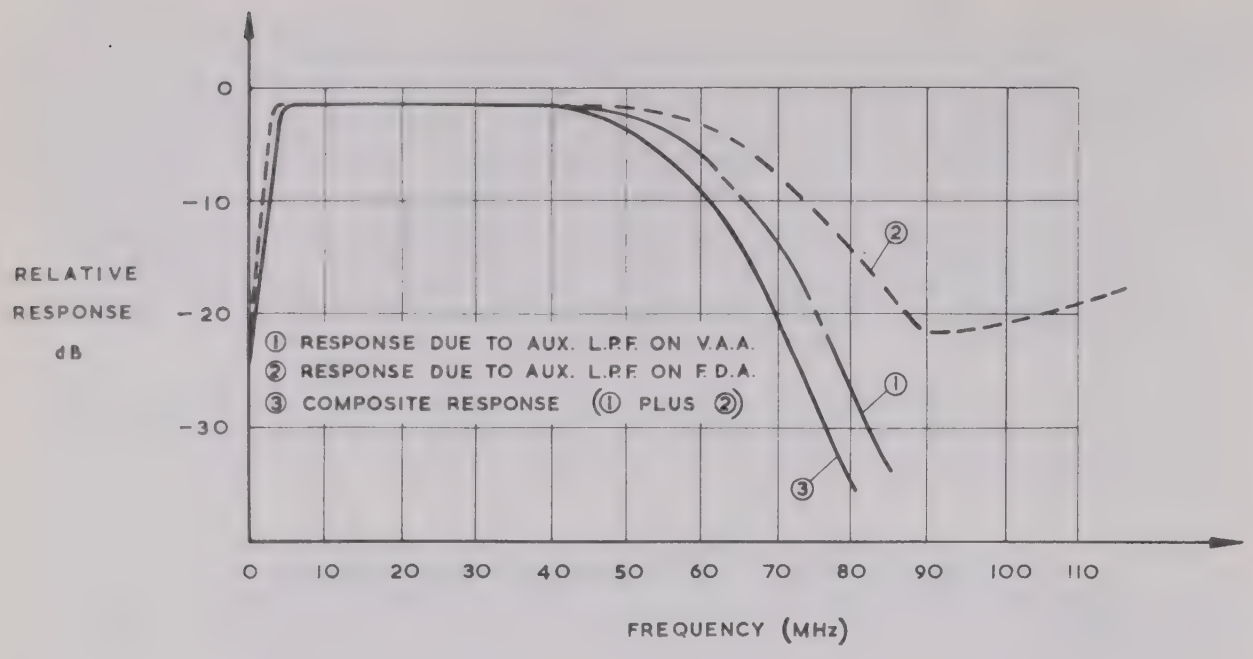


Fig. 2.3

Idealised Response of Converter on Range 1A (102 - 106 MHz)

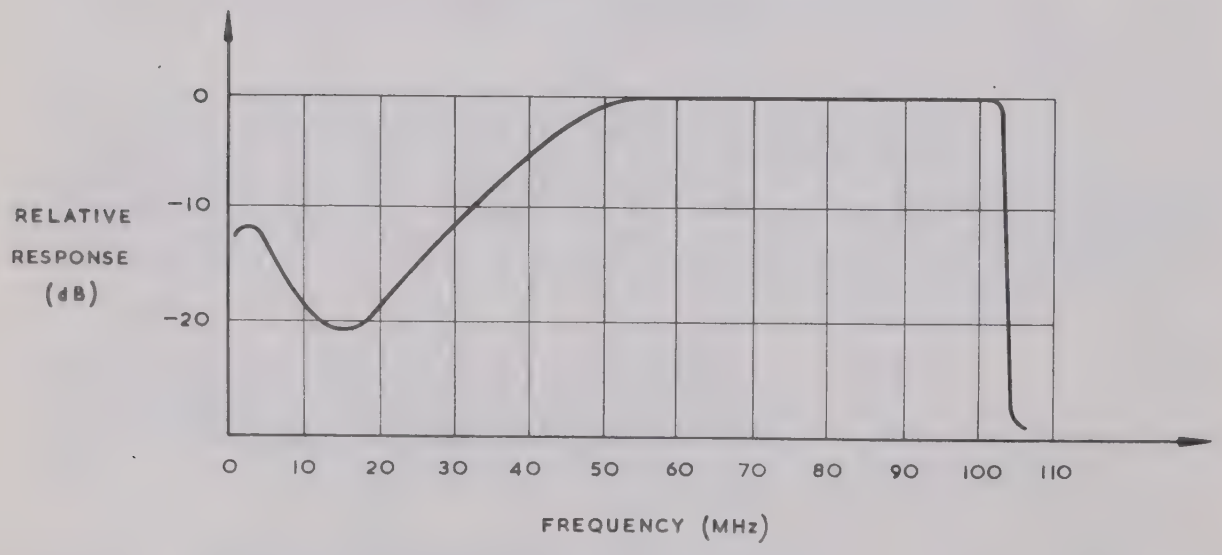


Fig. 2.4

Idealised Response of Converter on Range 1B (160 - 202 MHz)

2.3.97 Of the output frequencies listed, (3), (4), (5) and (6) are either (a) well outside the passband of the signal circuits or (b) too low in level to be of any significance. Outputs (1) and (2) however are likely to interfere with the operation of the counter and have to be suppressed. This is achieved with the aid of high-pass and low-pass auxiliary filters in the video amplifier and filter detector assemblies of the instrument as follows:-

2.3.98 In going from state zero (0 MHz) to state 4 (400 MHz), the shift register assembly 19-0006 scans the 100 MHz reference harmonic circuit in the harmonic generator assembly 19-0002 twice. On the first of these two scans, a d.c. level is fed from the shift register assembly (1) to the video amplifier assembly 19-0004 and (2) via resistor R1 to the filter detector assembly 19-0005. In each case the d.c. level input from the shift register assembly is used to switch into operation a low-pass auxiliary filter.

2.3.99 The overall effect of switching into circuit the low-pass auxiliary filters can be seen from the idealized response curves depicted in Fig. 2.3. Response curve (1) shows that signals to the counter are attenuated at 100 MHz by the low-pass auxiliary filter on the video amplifier assembly. The response as seen by the detector is modified not only by the low-pass auxiliary filter in the video amplifier assembly but also by the low-pass auxiliary filter in the filter detector assembly. The composite response seen by the detector is therefore always equal to or enclosed by the response as seen by the counter. At the frequencies stipulated in paragraph 2.3.96, any leakage of the reference harmonic f_o (100 MHz) or of the signal frequency f_s (104 MHz) would, under these conditions, be considerably reduced.

2.3.100 The composite response as seen by the detector stage ensures that a range-change action occurs before the signal level to the counter falls too low. The range-change action will take place in the region where the input signal frequency f_s is approximately 170 MHz.

2.3.101 On the second scan of the 100 MHz output circuit in the harmonic generator assembly, a d.c. level is fed from shift register assembly, edge-connection 16, to the filter detector assembly, pin 7. The effect of this, in the filter detector assembly, is to switch into the signal path the high-pass auxiliary filter.

2.3.102 The idealized response curve of Fig. 2.4 shows that the response now seen by the detector has a point of high attenuation in the region of 10 MHz. If the input frequency under measurement had been increased from its original value of 104 MHz to a new value of 180 MHz, then a range-change action would take place, resulting in a lock-on on the second scan of the 100 MHz output circuit of the harmonic generator assembly (range 1B) instead of the first (range 1A). Conversely, assuming the signal frequency was originally 180 MHz, then if it had subsequently been decreased in frequency to say 104 MHz, a range-change would take place in the region of

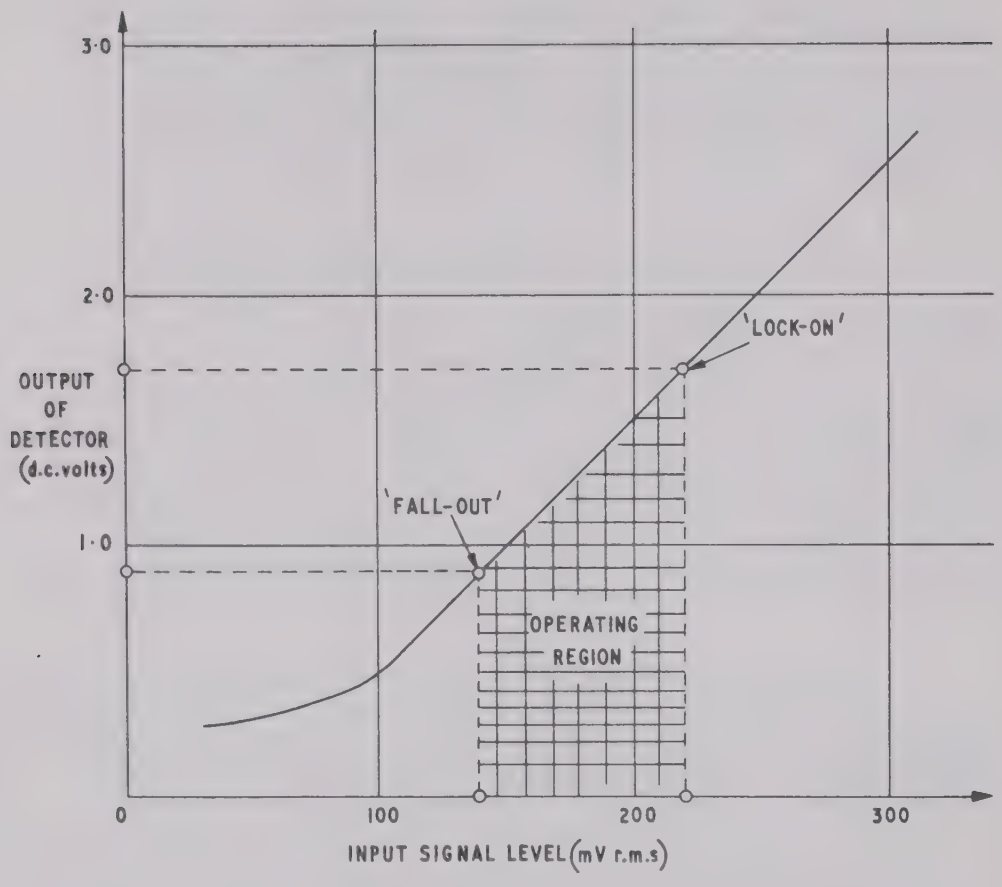


Fig. 2.5

(Detector Characteristic)

110 MHz. Under these conditions lock-on would occur on the first scan of the 100 MHz output circuit (range 1A) and not on the second (range 1B).

2.3.103 As can be seen from Fig. 2.5 the lock-on and fall-out points are on the linear part of the detector characteristic. Any unwanted signals of the type referred to in paragraphs 2.3.96 to 2.3.100 produce only a very low level signal at the input of the detector circuit and are thus confined to the lower part of the curve. Any d.c. output produced by the detector from such a signal will be below the level necessary to trigger the heterodyne frequency control circuits of the instrument to bring the system into lock.

2.3.104 Operation in the Range 2 to 102 MHz The heterodyne principle of operation of the r.f. circuits of the instrument is not applicable to signal frequencies between 2 and 102 MHz, such signals being suitable for measurement by the counter directly. The circuit action by which signals within this range are made available to the counter without change in frequency is as follows:-

2.3.105 The -12V power supply for the frequency multiplier assembly 19-0001 is controlled by a transistor switch in the shift register assembly 19-0006. Whenever the shift register assembly comes round to state zero (0 MHz) this supply is switched off thus rendering the frequency multiplier assembly totally inoperative. With the frequency multiplier assembly inoperative there can be no input to the harmonic generator assembly 19-0002 and therefore no reference harmonic input to the balanced mixer assembly 19-0003.

2.3.106 At the same time as the -12V power supply for the frequency multiplier assembly is switched off, a d.c. level of approximately -4V is fed from the shift register assembly, edge-connection 21, to the balanced mixer assembly, pin 21. In the mixer assembly this -4V level cuts off diodes D2 and D3 and switches on diode D1. Conditions in the balanced mixer assembly are now such that the signal frequency entering the assembly at pin 5 passes straight through R2, R4, D1 and C6 to output pin 18. On leaving the balanced mixer assembly the signal frequency is amplified in the video amplifier assembly 19-0004 to obtain an output at a suitable level for driving the counter. In the mixer assembly, resistors R2 and R4 provide sufficient attenuation to maintain a system gain consistent with that obtained when the mixer is operating on the other ranges.

2.3.107 Signal Gating In order that the frequency measurement display on the counter may be latched to the 'hundreds-of-megahertz' display on the converter, the output buffer stage preceding the output low-pass filter in the video amplifier assembly is gated. Control of the gated buffer stage is effected by the sequencing generator d.c. level output fed via edge-connection 10 on the sequence control assembly to pin 5 on the video amplifier assembly.

2.3.108 The gate is opened and the difference frequency fed through the low-pass filter to the counter when, at the end of the 'B' scan of the frequency control circuits, the d.c. output level at edge-connection 10 (0V) falls to approximately -5V. The gate remains open until such time as either (1) the input signal is disconnected or (2) its amplitude or its frequency changes sufficiently to cause the d.c. output level of the detector to fall below the second lower threshold level of the input trigger circuit on the sequence control assembly (point 'd' on Fig. 2.6).

2.3.109 Control Circuits

2.3.110 Introduction. Reference should be made throughout this section to the control sequence diagram Fig. 2.7 (page 31) and the functional outline block diagram Fig. 2.15 (following page 45).

2.3.111 General Operation. Assume that the AUTO/MANUAL switch on the front panel of the converter is set to AUTO. The output of the filter detector assembly is fed via the AUTO/MANUAL front panel control (SB) to the input trigger circuit on the sequence control assembly. When this output exceeds the first upper threshold level of the trigger circuit (point 'a' on Fig. 2.6) the circuit operates.

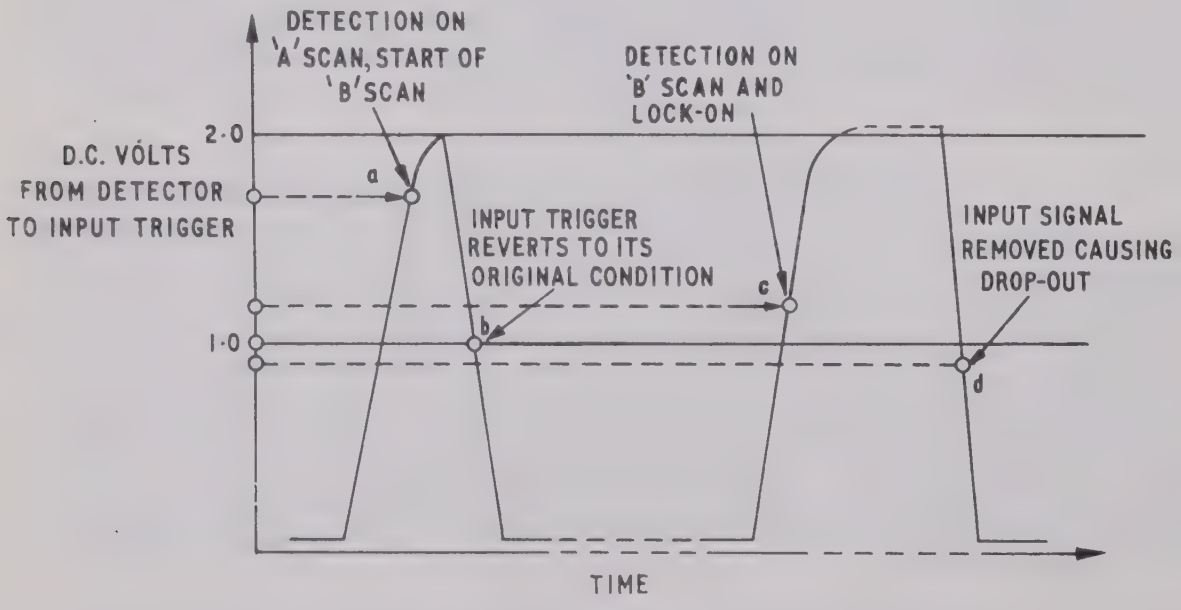


Fig. 2.6

Input Trigger Characteristic

2.3.112 The operation of the input trigger circuit produces a change in the level of its output to the sequencing generator, as a result of which the sequencing generator is inhibited. When the sequencing generator stops, its output to the and-gate changes in a negative direction. The input to the and-gate from the control flip-flop is also a negative d.c. level at this time and so the and-gate operates.

2.3.113 When the sequencing generator is inhibited, therefore, the change in level in its output to the and-gate is reproduced in the and-gate output to the delay generator. As soon as the level of the and-gate output changes, the delay generator is triggered. When the delay generator triggers, it produces a change in the level of its output to the main reset generator. Immediately this change in level of the delay generator output occurs, the main reset generator triggers.

2.3.114 Returning to the start of this sequence of events, i.e. the point at which the d.c. level output of the filter detector assembly exceeded the first upper threshold level of the input trigger circuit, it can be seen that the effect of this on the shift register assembly is twofold. First, since the sequencing generator has been inhibited, the shift register stops cycling. Secondly, since the main reset generator has been triggered, the shift register undergoes a reset action.

2.3.115 When the shift register resets, its output to the frequency multiplier assembly changes in a positive direction thereby rendering the multiplier inoperative. With the multiplier switched off, its output to the harmonic generator assembly falls to zero. Since the multiplier output is zero, the harmonic generator output to the balanced mixer assembly must also be zero.

2.3.116 The r.f. circuits of the instrument have thus changed over from (1) a condition in which the input signal frequency beats in the balanced mixer with the selected reference harmonic to produce a difference frequency response acceptable to the counter, to (2) one in which the signal frequency is fed to the balanced mixer on its own. The changeover from the first of these two conditions to the second causes the d.c. level at the output of the filter detector assembly to fall to zero. When this happens, a further train of events is triggered off as follows:-

2.3.117 When the d.c. level output of the filter detector assembly falls below the first lower threshold level of the input trigger (point 'b' on Fig. 2.6) this circuit reverts to its original condition. The change this brings about in the trigger output to the sequencing generator removes the inhibit from this circuit, thus allowing it to start up again. No further changes take place in the control system until the delay generator reverts to its original stable state. When this happens, the level of its output to the control flip-flop changes in a positive direction. This causes the control flip-flop to trigger, with the result that (1) its output to the and-gate changes in a positive

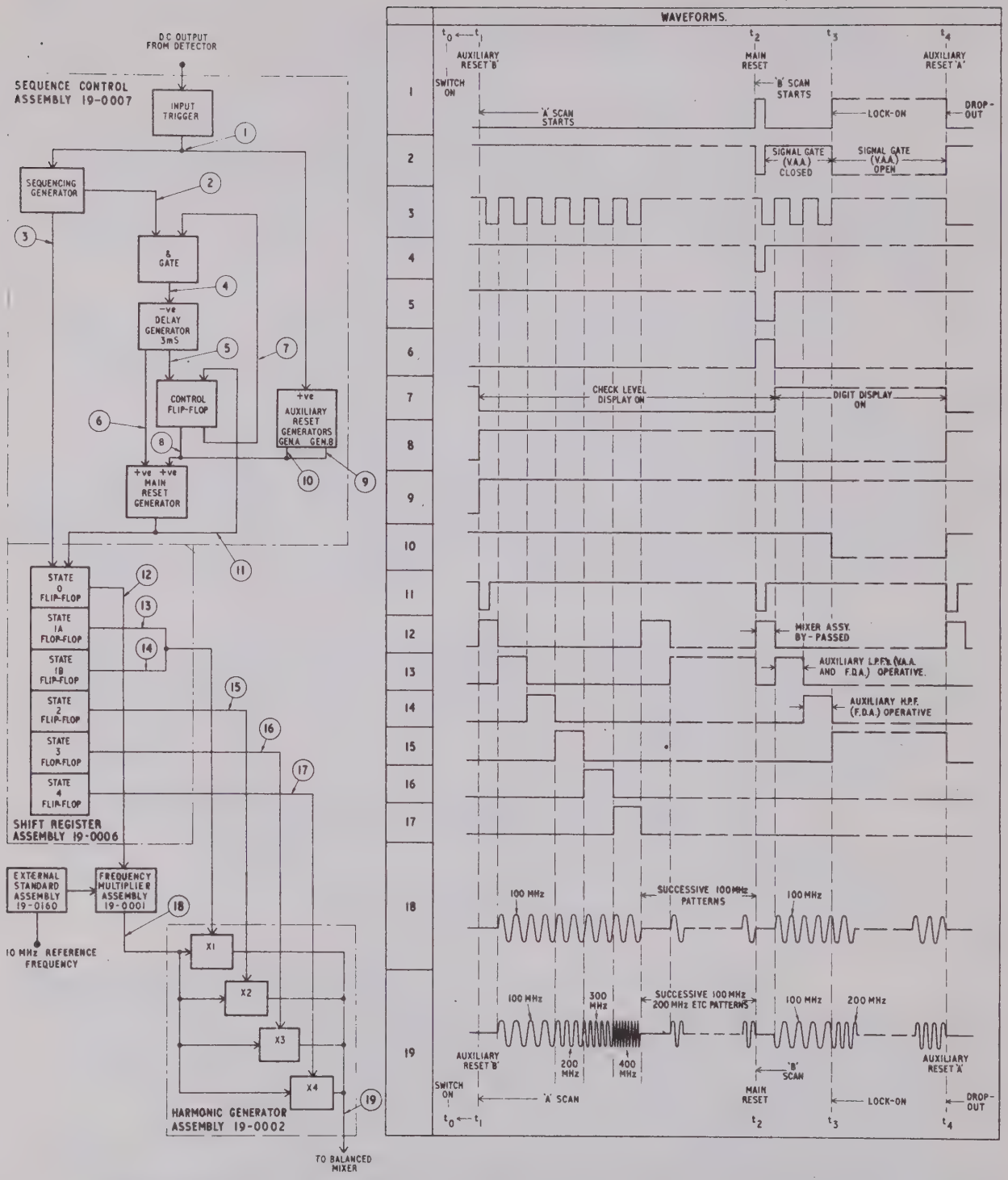
direction and (2) its output to the auxiliary reset generators common output line changes in a negative direction. Output (1) inhibits the and-gate and output (2) removes the inhibit on auxiliary reset generator 'A'. Output (2) is also fed back to the input trigger circuit where it lowers the threshold levels of the circuit (Fig. 2.6, points 'c' and 'd') thereby increasing its sensitivity.

2.3.118 Since the sequencing generator has started up again, its output to the shift register is restored. On the first positive-going edge of the sequencing generator output, the change in the shift register output to the frequency multiplier assembly effectively reconnects this to its -12V supply, thereby rendering the assembly operative again. This particular edge of the sequencing generator output also makes the next output of the shift register, i.e. the first of its two outputs to the X1 frequency multiplier in the harmonic generator assembly. The change in this output of the shift register switches the X1 frequency multiplier circuit on, thereby causing the harmonic generator output to the balanced mixer to change from 0 MHz to the reference harmonic at 100 MHz.

2.3.119 Succeeding positive-going edges of the sequencing generator output to the shift register change each of its other four outputs to the frequency multiplier circuits until the output fed to the balanced mixer is the reference harmonic immediately below the signal frequency. Assuming the signal frequency to be within the range 202 MHz to 302 MHz, the input to the mixer from the harmonic generator assembly would then be the reference harmonic at 200 MHz. The difference frequency response produced by beating this reference harmonic with the signal frequency ($f_s - f_o$) restores the d.c. level at the output of the filter detector assembly. When this d.c. level output exceeds the second upper threshold level of the input trigger circuit (Fig. 2.6, point 'c') the trigger circuit operates for the second time in the control cycle.

2.3.120 Conditions as far as the sequencing generator circuit is concerned are now the same as when the input trigger circuit was operated before, that is to say the sequencing generator is inhibited and its output to the and-gate is a negative d.c. level. This time, however, the and-gate circuit is inhibited, since the control flip-flop output to the gate is positive and not negative. As there is thus no and-gate output to trigger the delay generator and therefore no delay generator outputs to trigger the control flip-flop and the main reset generator, the state of these three control circuits remains unchanged. The control circuits have now locked on with the shift register stopped and the frequency multiplier and harmonic generator assemblies delivering to the balanced mixer assembly the reference harmonic at 200 MHz.

2.3.121 Auxiliary Reset 'A' Action Assume that, some time after the control circuits have locked on, the input signal is subject to a reduction in level sufficient to cause the output of the filter detector assembly to fall below the second lower threshold level of the input trigger circuit (point 'd' on Fig. 2.6). As soon as the output of the filter detector assembly



Control Sequence Waveforms for Automatic Frequency Converter

Input Signal Frequency Between 202 and 302 MHz.

Fig. 2.7

falls below this level, the input trigger circuit will revert to its original untriggered condition. The trigger output to the sequencing generator will then change in a negative direction, removing the inhibit from this circuit and thus allowing it to start up again.

2.3.122 The trigger circuit output is also fed to auxiliary reset generator 'A', which, since it is no longer inhibited by the control flip-flop (para. 2.3.117), inverts the trigger pulse. The inverted trigger pulse output of auxiliary reset generator 'A' triggers the main reset generator. The resulting reset pulse resets not only the shift register but also the control flip-flop.

2.3.123 Since the control flip-flop has been reset, its three outputs, (1) to the and-gate, (2) to the input trigger circuit and (3) to the auxiliary reset generators common output line, all revert to the levels shown. As the control flip-flop output to the and-gate changes back to a negative d.c. level, the gate circuit changes from its inhibited condition back to being primed. The change in the second of the two control flip-flop outputs has two effects. First, it restores the inhibit on the output of auxiliary reset generator 'A', thereby ensuring that this remains inoperative during normal operations of the input trigger circuit. Secondly, it reinstates the input trigger circuit threshold levels, and therefore the circuit sensitivity, to their original values. The control circuits will remain in this condition until such time as the level of the input signal is once again sufficient to cause the output of the filter detector assembly to rise above the level necessary to operate the input trigger circuit. When this happens, the sequence of events described in paras. 2.3.111 to 2.3.119 is repeated until finally the control circuits lock on again as described in para. 2.3.120.

2.3.124 Auxiliary Reset 'B' Action The main reset action which terminates the 'A' scan and starts off the 'B' scan is preceded by an auxiliary reset action similar to that described in paras. 2.3.122 and 2.3.123. The first of these two auxiliary reset actions differs from the second in that it is automatic and initiated solely by the action of auxiliary reset generator circuit 'B'.

2.3.125 Auxiliary reset generator 'B' triggers approximately 1 second after the converter is switched on. The reset 'B' output to the main reset generator changes in a positive direction thereby causing the main reset generator circuit to operate. The resulting reset pulse resets the shift register and the control flip-flop. With the control flip-flop in its reset condition, the input trigger, and-gate and auxiliary reset generator 'A' circuits are all in their correct initial states. This ensures that when the d.c. output level of the detector rises above the first upper threshold level of the input trigger circuit, the frequency control circuits operate in the manner described.

2.3.126 Manual Operation Assume that the AUTO/MANUAL switch on the front panel of the converter is set to MANUAL. Instead of being connected to the output of the filter detector assembly as before, the input of the input trigger is now connected via SB1 to the junction point of the two resistors, R1 and R2, connected across the +12V power supply. Since the potential at this point (+2.5V approximately) is greater than the first upper threshold level of the input trigger circuit (+1.5V approximately) the trigger circuit is held in its operated condition. The function of the sequencing generator, which circuit is now inhibited, is taken over by a differentiating circuit (R55 and C19 in assembly 19-0007) switched into circuit by SB2 and triggered (from the -12V supply) by means of the SHIFT/RECOUNT push-button switch SA. When the push-button is depressed, a single positive-going edge is fed to the shift register, causing it to advance from whichever state it happens to be in at the time to the next highest in the sequence.

2.3.127 A further function of the mode switch in manual operation is to ensure that the digit display power supply, which is controlled by the control flip-flop, is switched on. Normally, the -12V power supply for the digit lamps is switched on when the control flip-flop is triggered and off when it is reset. In the MANUAL position of the mode switch, the control flip-flop is held in its triggered condition (digit lamps -12V power supply ON) by SB3.

2.3.128 The SHIFT/RECOUNT switch SA also has its use in the automatic mode of operation of the converter, namely, as a reset control. In the AUTO position of the mode switch, depressing the push-button control disconnects the input trigger circuit from the output of the filter detector assembly. In the absence of an input, the trigger circuit reverts to its original (untriggered) condition, causing the frequency control circuits to reset in the manner described in paras. 2.3.121 to 2.3.123.

2.4 MAINTENANCE

2.4.1 REQUIRED TEST EQUIPMENT

2.4.2

(a) D.C. voltmeter with accuracy of ± 2% (e.g. Model 8 AVO)

(b) Oscilloscope: (e.g. Tektronix 453) Sensitivity: 5 mV/cm; Time Base: 0.01 μS/cm; Bandwidth: > 50 MHz

(c) Swept Oscillator (e.g. Rhode and Schwarz Polyskop II Type SWOB)

(d) R.F. Millivoltmeter (e.g. Airmec Type 301)

(e) Signal generator: (e. g. Airmec 201) Frequency range: 30 kHz - 30 MHz.

(f) VHF Signal Generator: (e. g. Boonton 3200A) Frequency range: 10 - 500 MHz. Output greater than 1V r. m. s.

2. 4. 3 REMOVAL OF INSTRUMENT COVERS

WARNING:- 115/230V A. C. IS EXPOSED WHEN THE INSTRUMENT COVERS ARE TAKEN OFF.

2. 4. 4. The general areas in which high voltages are present are identified by red dots, but care should be exercised at all times to reduce risk of electrical shock.

2. 4. 5 Before attempting to remove its covers ensure that the instrument is disconnected from the mains supply. Before re-connecting to the mains supply, check:-

(a) that the voltage taps are correctly positioned for the mains voltage available,

(b) that the fuses are of the correct rating as specified in Part 2. 1.

2. 4. 6 CHECKS AND ADJUSTMENTS

2. 4. 7 Preliminaries

2. 4. 8 Before carrying out any of the following checks or adjustments, ensure that:-

(1) POWER is connected but not switched on.

(2) AUTO/MANUAL switch is set to MANUAL.

(3) INPUT ATTENUATOR switch is set to 0dB.

(4) OUTPUT socket is terminated in 50 ohms and connected to a suitable 100 MHz counter.

(5) EXTERNAL STANDARD is connected to 10 MHz at a level of between 100 mV and 10V r. m. s.

2. 4. 9 When satisfied that the instrument is ready to use, switch on POWER and check that display indicator shows '0'.

2.4.10 Power Supplies

2.4.11 Power Supply Assembly 11-0033. This assembly is most conveniently checked with the instrument turned on to its side. Outputs of + 12V and - 12V (each ± 2%) should be obtained at the test points on the underside of the assembly. Adjustment is by means of potentiometer RV1 and RV2, both of which are accessible from the top side of the assembly.

2.4.12 Sequence Control and Logic Check

2.4.13 The operation of the sequence control and logic circuits of the instrument may be checked as follows:-

(1) Operate the SHIFT push-button and check that the front panel display changes in the following sequence:-

0, 1, 1, 2, 3, 4, 0, etc.

NOTE: The push-button should not be operated faster than once per second.

(2) Measure the control voltage levels and check the results against the figures shown in Table 2.2.

TABLE 2.2

CONTROL	Location Assembly	Pin No.	0	1A	Voltage 1B	2	3	4	Tolerance Volts
Mixer	BMA 19-0003	2	$-9\frac{1}{2}$	$+\frac{1}{2}$	$+\frac{1}{2}$	$+\frac{1}{2}$	$+\frac{1}{2}$	$+\frac{1}{2}$	$\pm\frac{1}{2}$
1st Aux LP	VAA 19-0004	1	0	$-4\frac{1}{2}$	0	0	0	0	$\pm\frac{1}{2}$
2nd Aux LP	FDA 19-0005	4	0	$-2\frac{1}{2}$	0	0	0	0	$\pm\frac{1}{2}$
Aux HP	FDA 19-0005	3	0	0	$-4\frac{1}{2}$	0	0	0	$\pm\frac{1}{2}$
Output Gate	VAA 19-0004	5	-6	-6	-6	-6	-6	-6	± 1
Multiplier inhibit	FMA 19-0001	1	0	-11	-11	-11	-11	-11	$\pm\frac{1}{2}$
Harmonic Generator Control	HGA 19-0002	(1	0	$-4\frac{1}{2}$	$-4\frac{1}{2}$	0	0	0	$\pm\frac{1}{2}$
		(2	0	0	0	$-4\frac{1}{2}$	0	0	$\pm\frac{1}{2}$
		(3	0	0	0	0	$-4\frac{1}{2}$	0	$\pm\frac{1}{2}$
		(4	0	0	0	0	0	$-4\frac{1}{2}$	$\pm\frac{1}{2}$

2.4.14 External Standard Assembly 19-0160

2.4.15 This assembly should provide a 10 MHz output, measured at output pin 6, of between 40 and 80 mV r.m.s. If this output is not obtained check that inductor L1 is adjusted for maximum 10 MHz signal amplitude.

2.4.16 Frequency Multiplier Assembly 19-0001

2.4.17 On all ranges except '0' this assembly should provide a 100 MHz output of between 0.4 and 0.6V r.m.s. If this output is not obtained adjust inductors L1 to L6 for maximum 100 MHz signal amplitude.

2.4.18 Filter Responses

2.4.19 Setting Up the Polyskop. The correct procedure for setting-up the Polyskop prior to checking the various filter responses is as follows:-

(1) Set zero line to zero graticule line.

(2) Set output attenuator to 15 dB.

(3) Set Y1 selector switch to probe input position.

(4) Set Y2 selector to EMF.

(5) Set frequency selector to 0.5 - 50 MHz.

(6) Connect r.f. output to converter input socket via coaxial earth pin.

(7) Place Probe on balanced mixer assembly input pin 5 and adjacent earth pin.

(8) Set Y1 and Y2 traces to be coincident, $\pm \frac{1}{2}$ dB over frequency range 0.5 - 50 MHz on graticule line 4.

WARNING:- Make NO further adjustments to Y2 gain as this now represents a reference for all measurements.

2.4.20 Mixer L - P Filter (19-0004).

(1) Connect the Probe to pin 4 and the adjacent pin.

(2) Operate the SHIFT push-button as necessary to set the converter to range '0'.

(3) Set the Polyskop frequency and output attenuator controls as follows:-

(i) Frequency - to 100 - 200 MHz.

(ii) Output Attenuator - adjust such that Y1 trace is coincident with Y2 ± 1 dB over frequency range 5 to 100 MHz.

(4) Check that the filter response is as shown in Fig. 2.8, and that the Polyskop attenuator setting is 26 dB ± 1½ dB.

(5) If the correct response is not obtained adjust C7, C17, C22 and C24 in conjunction with L1.

2.4.21 Video Amplifier Output L-P Filter (19-0004).

(1) Connect the Probe to pin 3 and the adjacent earth pin.

(2) Operate the SHIFT push-button to obtain range '0'.

(3) Set the Polyskop frequency and output attenuator controls as follows:-

(i) Frequency - to 100 - 200 MHz.

(ii) Output Attenuator - adjust such that Y1 trace is coincident with Y2 ± 1 dB over the frequency range 5 to 100 MHz.

(4) Check that the filter response is as shown in Fig. 2.9, also that the Polyskop attenuator setting is - 24 dB ± 1½ dB.

(5) If the required results are not obtained re-adjust C7, C17, C22 and C24 in conjunction with L3.

2.4.22 1st Aux. L-P Filter (19-0004)

(1) Verify that the Probe is connected to pin 3 and the adjacent earth pin.

(2) Operate the SHIFT push-button to obtain range 1A.

(3) Verify that the Polyskop frequency sweep control is set to 100 - 200 MHz.

(4) Set the Polyskop attenuator so that the Y1 trace is coincident with Y2 ± ½ dB over the frequency range 110 - 150 MHz.

(5) Check that the filter response is as shown in Fig. 2.10.

(6) If the response is not obtained as shown adjust L4 on the harmonic generator assembly 19-0002 (for coincidence of the Y1 and Y2 traces) and L2 in the video amplifier assembly.

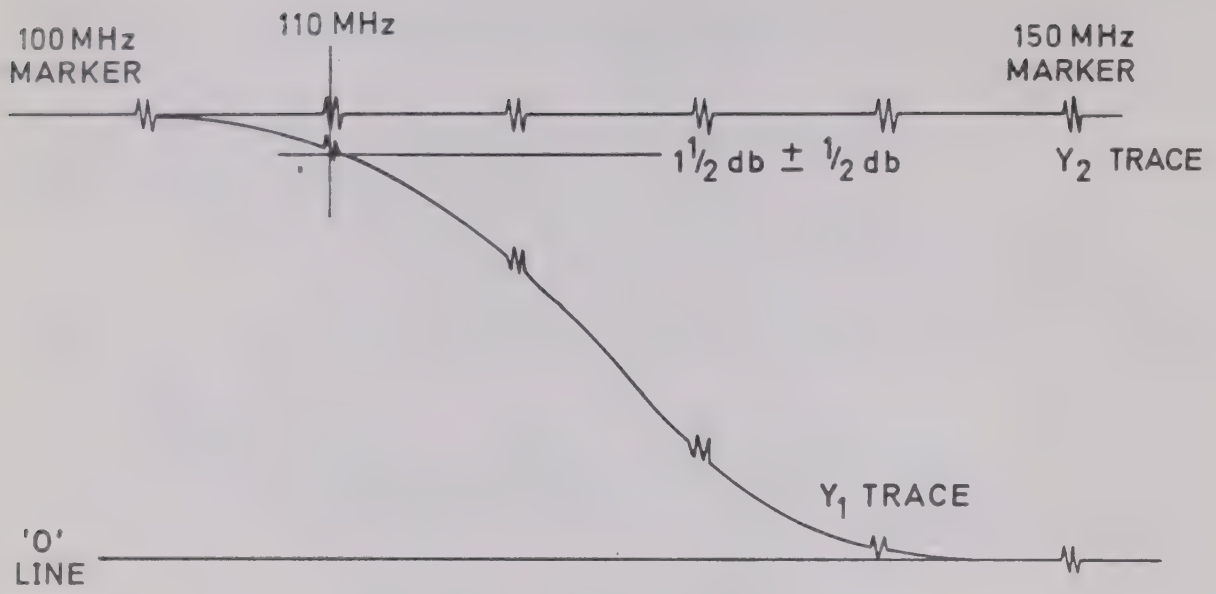

100 MHz
MARKER
110 MHz
150 MHz
MARKER
1½ db ± ½ db
Y2 TRACE
Y1 TRACE
'O'
LINE

Fig. 2.8

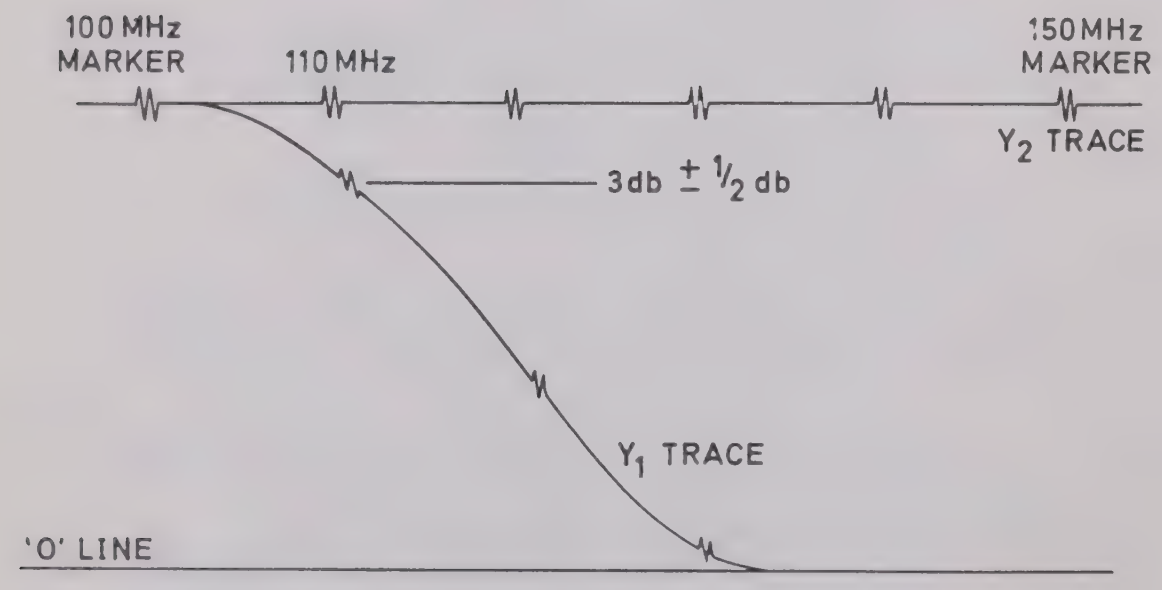

100 MHz
MARKER
110 MHz
150 MHz
MARKER
Y2 TRACE
3db ± ½ db
Y1 TRACE
'O' LINE

Fig. 2.9

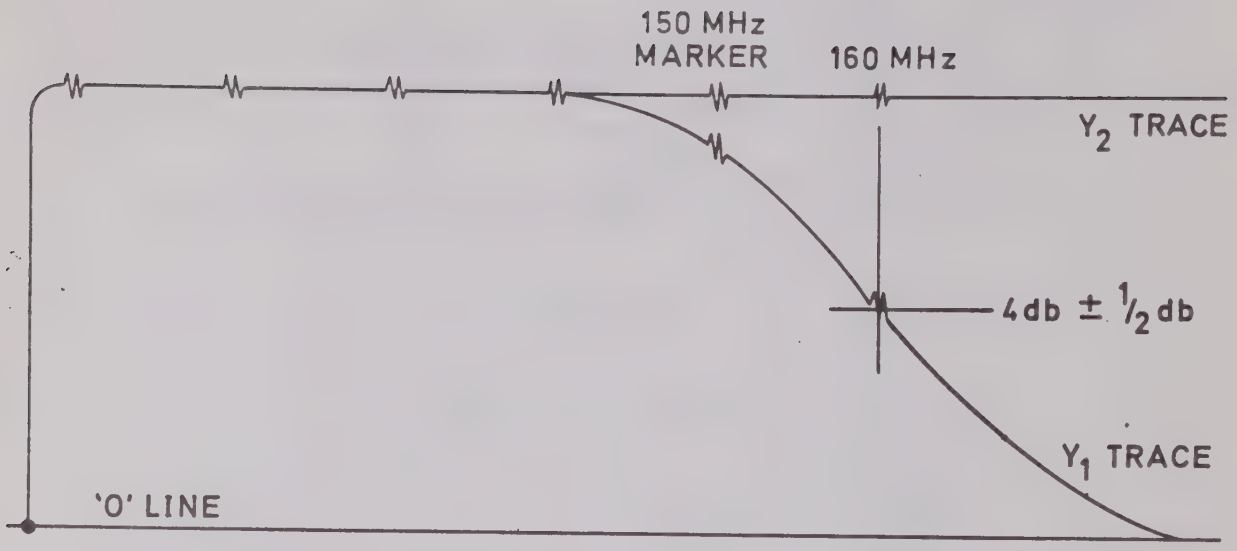


Fig. 2.10

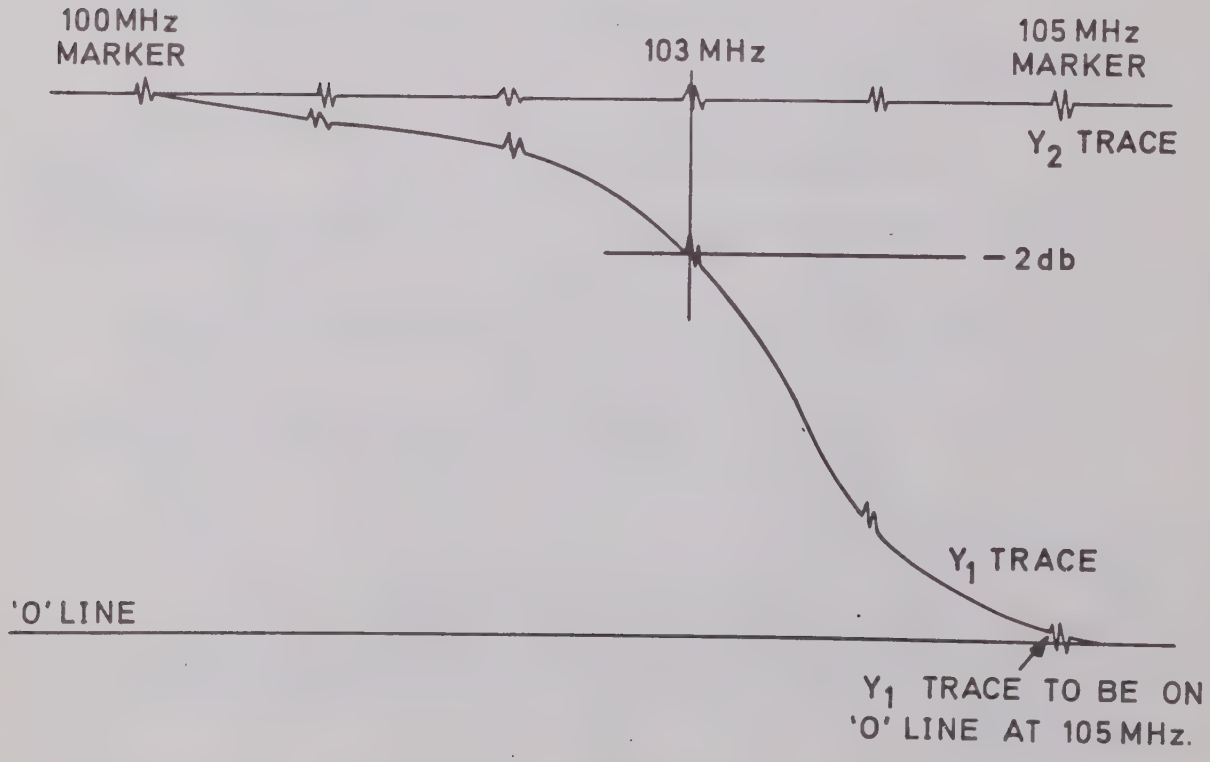


Fig. 2.11

2. 4. 23 Main L-P Filter (19-0005)

(1) Connect signal input of Probe to pin 5 and earth connection to pin 6.

(2) Operate the SHIFT push-button to obtain range '0'.

(3) Verify that the Polyskop frequency sweep control is set to 100 - 200 MHz.

(4) Set the Polyskop attenuator control so that Y1 trace is coincident with Y2 ± $\frac{1}{2}$ dB over the frequency range 5 - 100 MHz.

(5) Check that the filter response is as Fig. 2. 11, and that the Polyskop attenuator setting is - 29 dB ± $1\frac{1}{2}$ dB.

(6) If these results are not obtained adjust L1, L2, L3 and L4 in conjunction with C18.

2. 4. 24 Main H-P Filter (19-0005)

(1) Verify (1), (2) and (4) of the procedure for the main L-P filter.

(2) Set the Polyskop frequency sweep control to 0. 5 - 50 MHz.

(3) Check that the filter response is as shown in Fig. 2. 12.

(4) If the required response is not obtained adjust L5.

2. 4. 25 Mixer Balance (19-0003)

(1) Connect r. f. millivoltmeter to pin 3 and adjacent earth pin on the video amplifier assembly.

(2) Disconnect Polyskop from converter input socket and replace with a 50 ohm load.

(3) Operate SHIFT push-button as necessary to obtain range 1B.

(4) Check that R10 on the balanced mixer assembly is adjusted for minimum deflection on millivoltmeter and that the corresponding reading is less than 30 mV.

2. 4. 26 Overall System Gain

2. 4. 27 Harmonic Generator Assembly 19-0002

(1) Connect Polyskop r. f. output to converter input socket via a suitable coaxial cable.

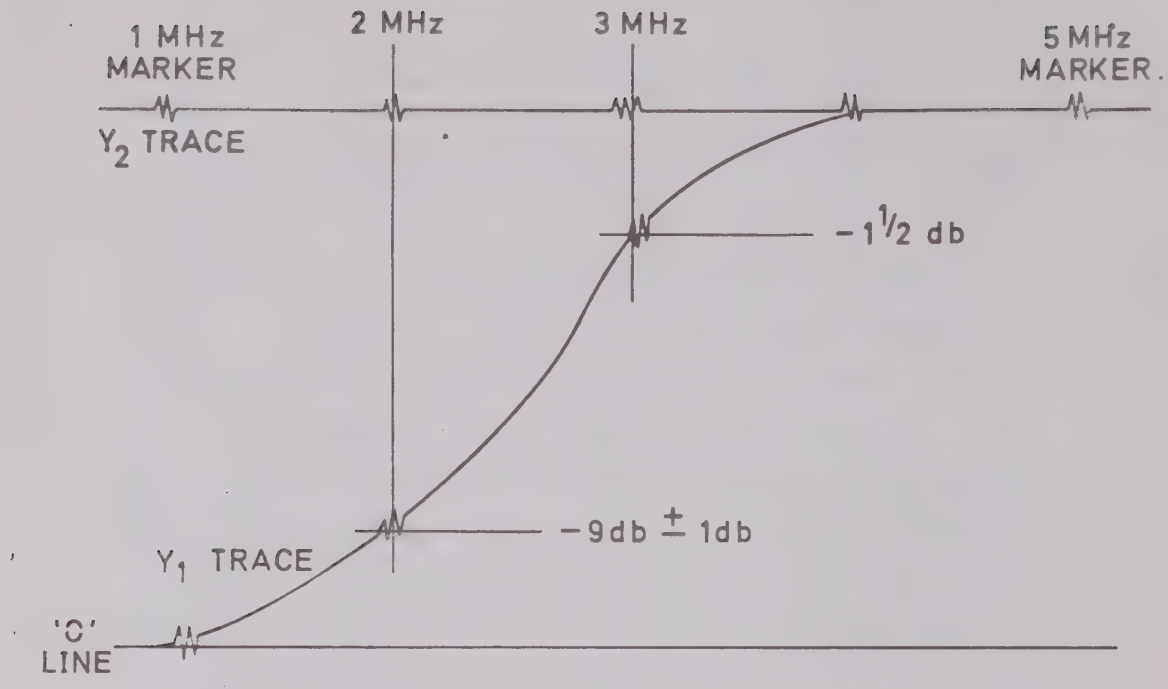


Fig. 2.12

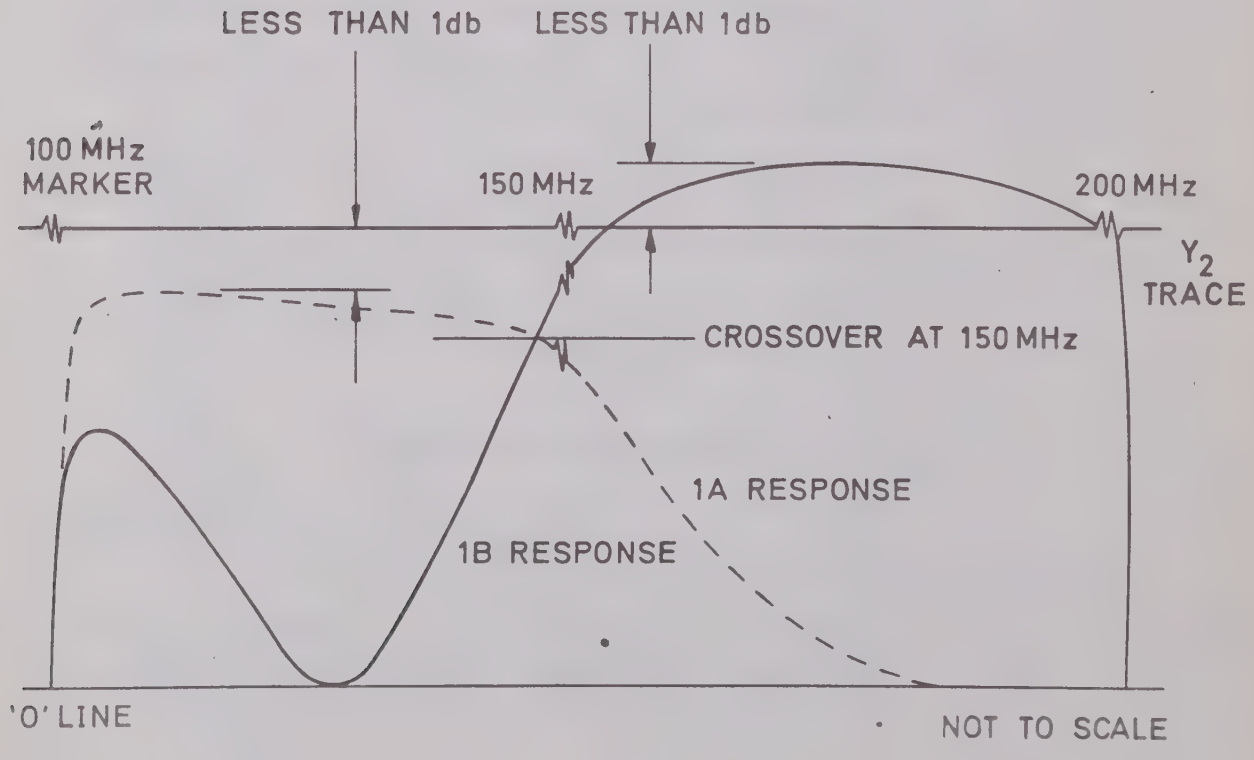


Fig. 2.13

(2) Check adjustments for each range in ascending order in accordance with Table 2. 3 and Fig. 2. 13.

(3) If it should be found necessary to make any adjustment(s) repeat sequence to check new setting(s).

NOTE: When making adjustments care should be taken that neither L1, L2 nor L3 is set past peak response.

2. 4. 28 Input Attenuator (Assembly 11-0116)

(1) Set Polyskop frequency to 50 - 100 MHz.

(2) Operate the SHIFT push-button to obtain range '0'.

(3) Note Polyskop output attenuator reading.

(4) Set converter INPUT ATTENUATOR switch to -20 dB.

(5) Adjust Polyskop output attenuator such that Y1 trace is again coincident with Y2 and note new reading.

(6) Check that difference between first and second reading is 20 dB $\pm 1\frac{1}{2}$ dB.

2. 4. 29 Detector Check (Assembly 19-0005)

(1) Connect signal generator to converter input socket.

(2) Set MANUAL/AUTO switch on converter to AUTO.

(3) With no input from signal generator check that display indicator shows 'CHECK LEVEL'.

(4) Connect oscilloscope to output pin 8 (assembly 19-0005) and earth to casting.

(5) Set oscilloscope sensitivity to $\frac{1}{2}$ volt per division.

(6) With no input to converter check the d. c. level displayed on oscilloscope; this should be 0 $\pm \frac{1}{2}$V.

(7) Set trace as reference.

2. 4. 30 Trigger Adjustment (Assembly 19-0007)

(1) With the input frequency at 90 MHz, increase the signal level until maximum voltage on oscilloscope trace has increased to 1. 5V above reference.

(2) Check that system is in 'lock', i. e. display indicator showing '0'. If system is out of 'lock', i. e. display showing 'CHECK LEVEL', adjust potentiometer RV1.

TABLE 2.3

OPERATE SHIFT/RESET FOR RANGE	POLYSKOP ADJUSTMENT		INSTRUMENT ADJUSTMENT H. G. A. 19-0002			
	FREQUENCY MHz	OUTPUT ATTENUATOR dB	COMPONENTS	ACCOMPLISHMENT	FREQUENCY MHz	TOLERANCE dB
0	0.5 - 50 and 50 - 100	Remain as positioned for 2.4.18	Remain as adjusted for 2.4.18	Coincidence of Y.1 with Y.2 trace	5 - 100	± ½
1A	100 - 200	Reduce 2dB from 0 range setting	L.4	ditto	See Fig. 2.13	± ½
1B	100 - 200	----	----	Response as Fig. 2.13		
2	200 - 300	As for 1A	1st C1, C2 2nd L3	1st Maximum output of Y.2 trace Adjustment thru casting base via holes in SRA 19-0006. 2nd Coincidence of Y.1 to Y.2 trace.	205 - 300	± ½
3	300 - 400	As for 1A	1st C3, C4 2nd L2		305 - 400	± ½
4	400 - 500	As for 1A	1st C5, C6 2nd L1		405 - 500	± ½

(3) Set input signal until maximum voltage displayed on oscilloscope is 0.7V above reference.

(4) Check that system is now out of 'lock'. If system is still in 'lock', adjust potentiometer RV2.

(5) Should it be found necessary to make any adjustment(s) the above operations should be repeated to check the new control setting(s).

NOTE: Fig. 2.14 shows the detector waveform for an input of 90 MHz before 'lock-on' occurs.

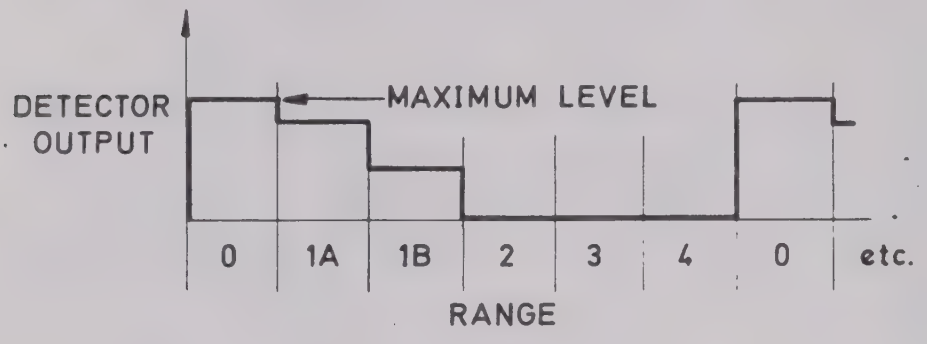


Fig. 2.14

2.4.31 Complete Instrument Check

2.4.32 Performance with High Input Level

(1) Set signal generator output to 1 volt and frequency as set out in Table 2.4.

NOTE: Frequency setting accuracy is not critical; the figures quoted serve only as a guide. The important requirement is that as the range is advanced by one, then the frequency output, as displayed on the counter connected to the converter output socket should decrease by exactly 100 MHz. If this does not happen check the following:-

(i) Alignment of frequency multiplier assembly 19-0001 (Section 2.4.16).

(ii) Mixer balance (Section 2.4.25).

(iii) Setting of tuning slugs in inductors L1, L2 and L3 of harmonic generator assembly 19-0002 (Section 2.4.27).

TABLE 2.4

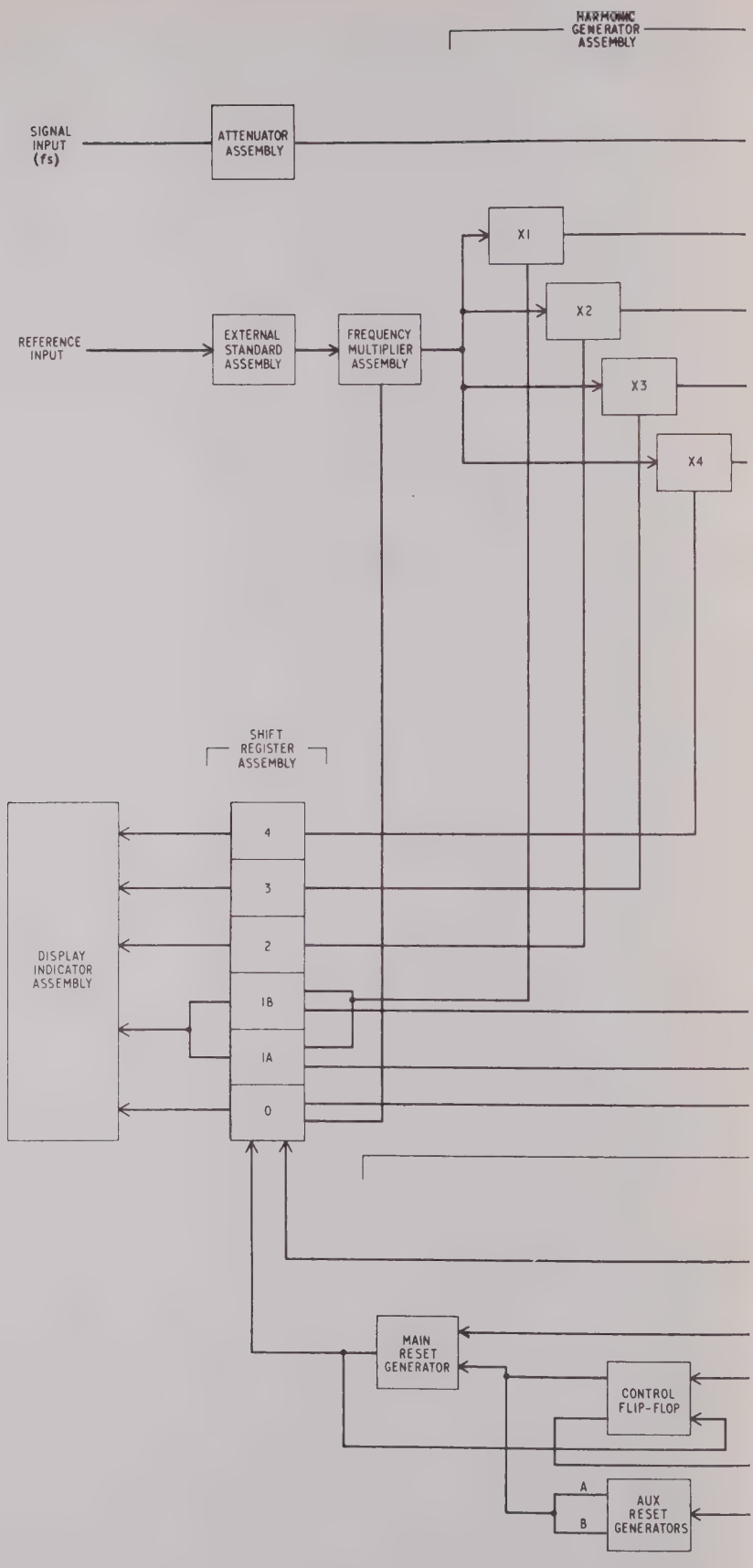
Range	0	1A	1B	2	3	4
Input Frequency (MHz)	102	102 103	130 202	202 302	302 402	402
Counter Reading (MHz)	102	2 30	30 102	2 102	2 102	2

(2) Set AUTO/MANUAL switch to AUTO.

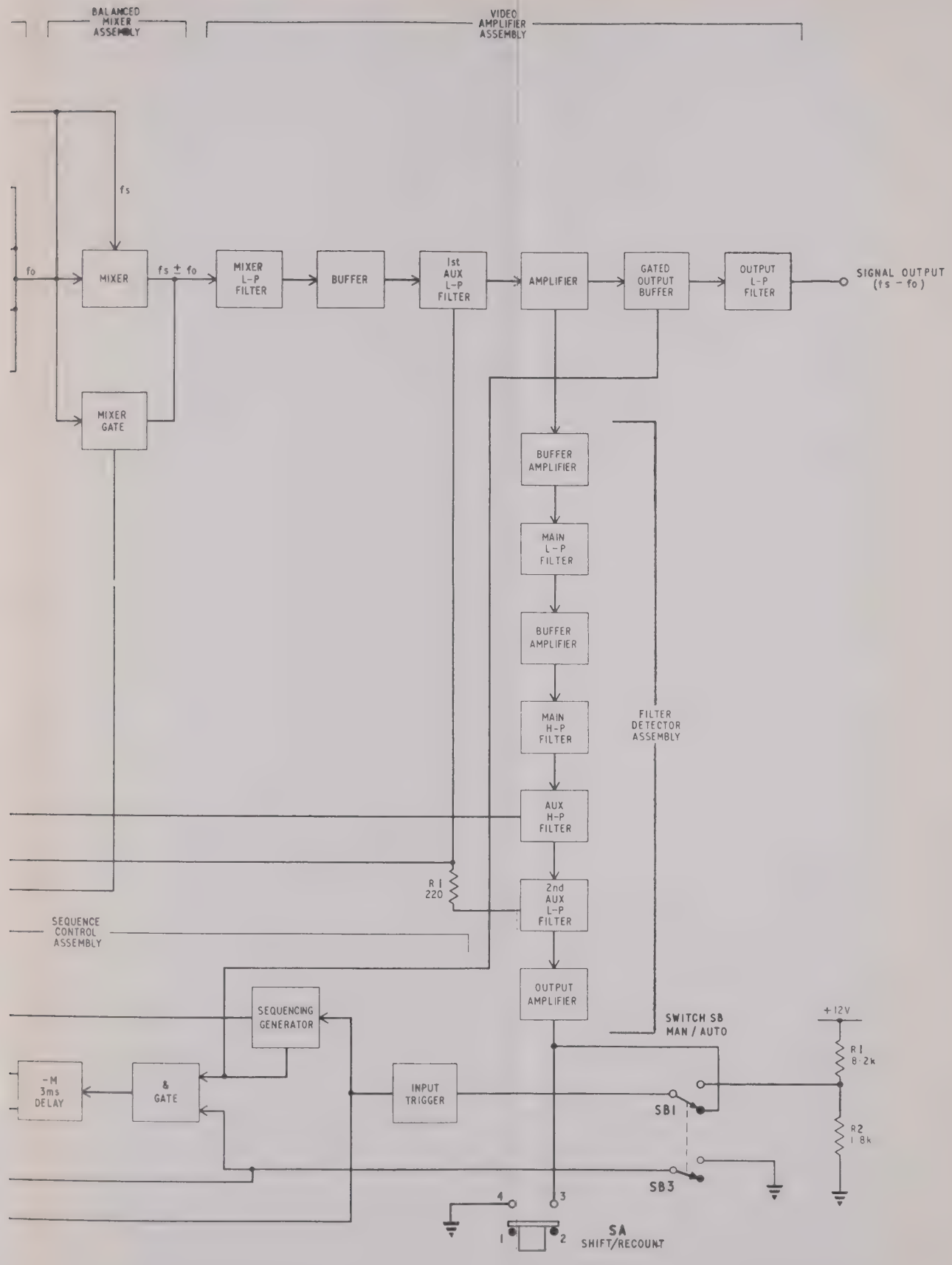
(3) With the input set at 1 volt, sweep the input frequency from 10 MHz to 500 MHz, checking that correct 'lock' is obtained at all frequencies and that the correct digit is shown on the display indicator.

2.4.33 Sensitivity Check

2.4.34 Repeat preceding sweep measurement with a constant input level of 70 mV r.m.s., checking that correct 'lock' and digit indication is obtained.


HARMONIC GENERATOR ASSEMBLY
SIGNAL INPUT (fs)
ATTENUATOR ASSEMBLY
X1
X2
X3
X4
REFERENCE INPUT
EXTERNAL STANDARD ASSEMBLY
FREQUENCY MULTIPLIER ASSEMBLY
SHIFT REGISTER ASSEMBLY
DISPLAY INDICATOR ASSEMBLY
4
3
2
1B
1A
0
MAIN RESET GENERATOR
CONTROL FLIP-FLOP
A
B
AUX RESET GENERATORS

Funct



tional Outline Block Diagram : SA. 565

Fig. 2. 15

PART 3

PARTS LIST

Part No.	Description	Rat.	Tol %	Value	Qty	Component References	Vendor
			+80	500 MHz A.F.C. PACKAGE No. 11-0000			
21-6500	Capacitor Feed Through		-20	1000	18	C1 to C18 inc.....	Erie K2600/361-101
23-8000	Bead Ferrite				1	X1.....	Mullard FX 1242
23-3005	Socket B.N.C.			50Ω	1		Amphenol UG-1094/U
				MAIN CHASSIS ASSEMBLY No. 11-0001			
20-0100	Resistor Composition 1/10W		10	10	1	R3.....	Erie 15
20-0182	Resistor Composition 1/10W		10	1.8k	1	R2.....	Erie 15
20-0822	Resistor Composition 1/10W		10	8.2k	1	R1.....	Erie 15
23-1005	Indicator				1		K.G.M. M4
23-4002	Switch Slide				1	SB.....	Plessey S6
23-4003	Switch Push Button				1	SA.....	Painton 401404
23-4004	Switch Toggle				1	SC.....	Arrow BT33
23-5048	Edge Connector (23-way)				1		Carr Fastener 83/487-22
23-5034	Edge Connector (12-way)				1		Pressac 60/066/FR
				POWER SUPPLY ASSEMBLY, MODEL 1, No. 11-0033			
17-4004	Transformer				1	T1.....	Racal Instr.
21-0506	Capacitor Electrolytic or	40V		2500μ	2	C2, C3.....	Plessey CE12135/13
21-0510	Capacitor Electrolytic or	40V		2500μ			Mullard C431BR/G2500
21-0516	Capacitor Electrolytic	25V		2500μ			Hunts KA 2051
22-6011	Transistor npn silicon				2	Q1, Q3.....	R.C.A. 40250
23-0004	Fuse Link	0.5A			2	F1, F2.....	Bulgin F270
23-0007	Fuse Link	1.5A			2	F3, F4.....	Bulgin F270
23-3032	Socket 5 x 2 Way - Selector				1		Spear Eng. S177
23-3035	Plug Shorting - Red				1		Spear Eng. S491
23-3036	Receptical Male 3 Pins Power				1	PL1.....	Bulgin P429
23-5036	Connector P.C. Board				2		Ether KKM. 15-S-H
				ATTENUATOR ASSEMBLY No. 11-0092			
17-0004	Rotary Switch				1	SA.....	Racal Instr.
23-3046	B.N.C. Bulkhead Jack UG909B/U				1		Greenpar GE 35042C10

Part No.	Description	Rat.	Tol. %	Value	Qty	Component References	Vendor
				FREQUENCY MULTIPLIER ASSEMBLY NO.19-0001			
17-3000	Coil Assembly				1	L1	Racal Instr.
17-3001	Coil Assembly				1	L2	Racal Instr.
17-3002	Coil Assembly				1	L3	Racal Instr.
17-3003	Coil Assembly				1	L4	Racal Instr.
17-3004	Coil Assembly				1	L5	Racal Instr.
17-3005	Coil Assembly				1	L6	Racal Instr.
	RESISTORS						
20-0100	Composition	1/10W	10	10	1	R20	Erie 15
20-0152	Composition	1/10W	10	1.5k	1	R6	Erie 15
20-0220	Composition	1/10W	10	22	2	R4, R6	Erie 15
20-2152	Metal Oxide	$\frac{1}{4}$W	5	1.5k	4	R2, R7, R12, R17	Erie MO4
20-2392	Metal Oxide	$\frac{1}{4}$W	5	3.9k	4	R3, R8, R13, R18	Erie MO4
20-2681	Metal Oxide	$\frac{1}{4}$W	5	680	4	R5, R10, R15, R19	Erie MO4
20-2120	Metal Oxide	$\frac{1}{4}$W	5	12	1	R14	Erie MO4
	CAPACITORS						
21-1565	Ceramic	150V	10	22p	1	C17	Erie YD
21-1573	Ceramic	150V	10	100p	2	C7, C13	Erie YD
21-1590	Ceramic	150V	10	210p	2	C1, C4	Erie YD
21-1591	Ceramic	100V	- 20 + 80	0.01	8	C3, C5, C9, C11, C15, C16, C19, C20	Erie 801
21-2507	Silver Mica	300V	5	27p	2	C14, C18	Erie EDM 15 J
21-2521	Silver Mica	300V	5	100p	1	C6	Erie EDM 15 J
21-2525	Silver Mica	300V	5	150p	2	C8, C12	Erie EDM 15 J
21-2537	Silver Mica	300V	5	470p	1	C2	Erie EDM 15 J
21-1505	Ceramic		10	5.6p	1	C10	Erie P 100
21-1551	Ceramic		10	0.1	1	C21	
	DIODES						
22-1004	Silicon (Specially Selected)				1	D1	Microwave Ass. 1N416 BN
	TRANSISTORS						
22-6001	Silicon npn				4	Q1, Q2, Q3, Q4	Texas D1559
23-8000	Bead Ferrite				9		Mullard FX 1242

Part No.	Description	Rat.	Tol. %	Value	Qty	Component References	Vender
				HARMONIC GENERATOR ASSEMBLY NO.19.0002			
17-3006	Coil Assembly				1	L4	Racal Instr.
17-3007	Coil Assembly				3	L1, L2, L3	Racal Instr.
17-3008	Coil Assembly				2	L5, L6	Racal Instr.
17-3009	Coil Assembly				2	L7, L8	Racal Instr.
17-3010	Coil Assembly				2	L9, L10	Racal Instr.
	RESISTORS						
20-0103	Composition	1/10W	10	10k	4	R16, R18, R20, R22	Erie 15
20-0121	Composition	1/10W	10	120	1	R14	Erie 15
20-0152	Composition	1/10W	10	1.5k	4	R17, R19, R21	Erie 15
20-0220	Composition	1/10W	10	22	3	R4, R7, R10	Erie 15
20-0472	Composition	1/10W	10	4.7k	3	R6, R9, R12	Erie 15
20-0680	Composition	1/10W	10	68	1	R23	Erie 15
20-2152	Metal Oxide	$\frac{1}{4}$W	5	1.5k	1	R2	Erie MO4
20-2392	Metal Oxide	$\frac{1}{4}$W	5	3.9k	1	R3	Erie MO4
20-2681	Metal Oxide	$\frac{1}{4}$W	5	680	3	R5, R8, R11, R15	Erie MO4
20-0820	Composition	1/10W	10	82	1	R13	Erie 15
	CAPACITORS						
21-1569	Ceramic	150V	10	47	1	C14	Erie YD
21-1571	Ceramic	150V	10	68	2	C13, C15	Erie YD
21-1573	Ceramic	150V	10	100	2	C1, C16	Erie YD
21-1563	Ceramic	150V	10	15	1	C17	Erie YD
21-1585	Ceramic	150V	10	1000	7	C2, C4, C6, C7, C9, C10, C11	Erie YD
21-2580	Silver Mica	500V	5	47	4	C5, C3, C8, C12	Erie 651-004
21-1591	Ceramic	100V	- 20 + 80	0.01μ	1	C18	Erie 801
21-1568	Ceramic	100V		39	1	C19	Erie YD
21-6001	Trim	150V		0.5-5	6	CT1, CT2, CT3, CT4, CT5, CT6	Erie CT52G
	DIODES						
22-0000	Germanium				2	D1, D3	Mullard OA47
22-1002	Silicon				2	D5, D7	Hughes HS9006
	or						
22-1021	Silicon						Hughes HS9007
22-1004	(Specially Selected)				3	D2, D4, D6	Microwave Ass. IN416 BN

Part No.	Description	Rat.	Tol. %	Value	Qty	Component References	Vendor
	TRANSISTORS						
22-6001	Silicon npn				4	Q1, Q2, Q3, Q4	Texas D1559
	BALANCED MIXER ASSEMBLY NO. 19-0003						
	RESISTORS						
20-0100	Composition	1/10W	10	10	1	R3	Erie 15
20-0102	Composition	1/10W	10	1k	1	R7	Erie 15
20-0103	Composition	1/10W	10	10k	3	R8, R12, R13	Erie 15
20-0223	Composition	1/10W	10	22k	2	R9, R11	Erie 15
20-0680	Composition	1/10W	10	68	2	R5, R6	Erie 15
20-2221	Metal Oxide	$\frac{1}{4}$W	5	220	1	R2	Erie MO4
20-2560	Metal Oxide	$\frac{1}{4}$W	5	56	1	R4	Erie MO4
20-2680	Metal Oxide	$\frac{1}{4}$W	5	68	1	R1	Erie MO4
20-6546	Variable		20	10k	1	R10	Plessey MP (Dealer) Printed Ct.
	CAPACITORS						
21-1505	Ceramic	500V	10	5.6	1	C1	Erie 831
21-1565	Ceramic	150V	10	22μ	1	C2	Erie YD
21-1591	Ceramic	100V	+80 -20	0.01μ	4	C3, C4, C5, C6	Erie 801
	DIODES						
22-1024	Silicon(Matched pair)				2	D2, D3	Hewlett-Packard HP 2912
22-1018	Silicon				1	D1	Hewlett-Packard HPA 2900
23-7027	Choke			.22μH	1	L1	Cambion 2960/22/3
	or						
23-7004	Choke						Painton 58/10/0001/10
23-8001	Core-Ferrite				2	T1, T2	Mullard FX2249

Part No.	Description	Rat.	Tol. %	Value	Qty.	Component References	Vendor
				VIDEO AMPLIFIER ASSEMBLY NO. 19-0004			
	RESISTORS						
20-0101	Composition	1/10W	10	100	1	R13	Erie 15
20-0103	Composition	1/10W	10	10k	1	R7	Erie 15
20-0150	Composition	1/10W	10	15	1	R2	Erie 15
20-0151	Composition	1/10W	10	150	1	R8	Erie 15
20-0152	Composition	1/10W	10	1.5k	1	R10	Erie 15
20-0220	Composition	1/10W	10	22	1	R31	Erie 15
20-0331	Composition	1/10W	10	330	1	R12	Erie 15
20-0470	Composition	1/10W	10	47	1	R31	Erie 15
20-0392	Composition	1/10W	10	3.9k	2	R18, R23	Erie 15
20-0471	Composition	1/10W	10	470	1	R11	Erie 15
20-0472	Composition	1/10W	10	4.7k	1	R28	Erie 15
20-0560	Composition	1/10W	10	56	1	R30	Erie 15
20-0680	Composition	1/10W	10	68	1	R1	Erie 15
20-0681	Composition	1/10W	10	680	2	R32, R9	Erie 15
20-0820	Composition	1/10W	10	82	4	R6, R14, R19, R24	Erie 15
20-0822	Composition	1/10W	10	8.2k	1	R29	Erie 15
20-0221	Composition	1/10W		220	1	R33	Erie 15
20-2220	Metal Oxide	$\frac{1}{4}$W		22	2	R4, R26	Erie MO4
20-2221	Metal Oxide	$\frac{1}{4}$W		220	2	R15, R20	Erie MO4
20-2271	Metal Oxide	$\frac{1}{4}$W		270	2	R3, R25	Erie MO4
20-2680	Metal Oxide	$\frac{1}{4}$W		68	2	R16, R21	Erie MO4
20-3681	Metal Oxide	$\frac{1}{2}$W		680	4	R5, R17, R22, R27	Erie MO5
	CAPACITORS						
21-1591	Ceramic			0.01μ	16	C4, C5, C6, C8, C11, C13, C14, C16, C18, C19, C21, C23, C25, C27, C28, C29	Erie 801
21-1601	Ceramic			6.8	1	C10	Erie YD
21-1602	Ceramic			8.2	1	C2	Erie YD
21-1603	Ceramic			15	1	C32	Erie YD
21-1604	Ceramic			32	4	C20, C1, C3, C15	Erie YD
21-1606	Ceramic			39	2	C31, C33	Erie YD
21-1607	Ceramic			47	2	C9, C12	Erie YD
21-6000	Trimmer	10/40			4	C7, C17, C22, C24	Steatite Ins 10S-Triko-06

Part No.	Description	Rat.	Tol. %	Value	Qty.	Component References	Vendor
	DIODES						
22-1002	Silicon				3	D1, D2, D3	Hughes HS9006
	TRANSISTORS						
22-6001	Silicon npn				5	Q1, Q2, Q3, Q4, Q5	Texas D1559
17-3011	Coil Assembly				1	L3	Racal Instr.
17-3022	Coil Assembly				1	L2	Racal Instr.
17-3023	Coil Assembly				1	L1	Racal Instr.
	FILTER DETECTOR ASSEMBLY NO. 19-0005						
17-3012	Coil Assembly				2	L1, L3	Racal Instr.
17-3013	Coil Assembly				2	L2, L4	Racal Instr.
17-3014	Coil Assembly				1	L5	Racal Instr.
17-3015	Coil Assembly				1	L9	Racal Instr.
	RESISTORS						
20-0101	Composition	1/10W	10	100	2	R1, R13	Erie 15
20-0103	Composition	1/10W	10	10k	2	R14, R11	Erie 15
20-0151	Composition	1/10W	10	150	1	R6	Erie 15
20-0181	Composition	1/10W	10	180	2	R12, R15	Erie 15
20-0220	Composition	1/10W	10	22	1	R21	Erie 15
20-0330	Composition	1/10W	10	33	2	R3, R9	Erie 15
20-0470	Composition	1/10W	10	47	1	R5	Erie 15
20-0680	Composition	1/10W	10	68	1	R7	Erie 15
20-0681	Composition	1/10W	10	680	1	R10	Erie 15
20-2101	Metal Oxide	$\frac{1}{4}$W	5	100	1	R8	Erie 15
20-2681	Metal Oxide	$\frac{1}{4}$W	5	680	1	R4	Erie 15
20-2271	Metal Oxide	$\frac{1}{4}$W	5	270	1	R2	Erie MO4
20-4018	Metal Oxide	$\frac{1}{4}$W	2	10k	1	R16	Erie MO4
20-4021	Metal Oxide	$\frac{1}{4}$W	2	15k	1	R19	Erie MO4
20-4023	Metal Oxide	$\frac{1}{4}$W	2	130K	1	R18	Erie MO4
20-4024	Metal Oxide	$\frac{1}{4}$W	2	1.2k.	1	R20	Erie MO4
20-3474	Metal Oxide	$\frac{1}{2}$W	5	470k	1	R17	Welwyn MR5

Part No.	Description	Rat.	Tol. %	Value	Qty.	Component References	Vendor
	CAPACITORS						
21-1500	Ceramic	500V	10	2.2	1	C14	Erie 831
21-1552	Ceramic	12V	10	0.1μ	2	C2, C15	Centralab DA476-001E
21-1573	Ceramic	150V	10	100	1	C5	Erie YD
21-1591	Ceramic	100V	+ 80 - 20	0.01μ	10	C1, C3, C4, C16, C21, C23, C24, C26, C27, C29	Erie 801
21-2501	Silver Mica	300V	5	12	2	C6, C10	Erie EDM 15 J
21-2505	Silver Mica	300V	5	22	4	C8, C12, C13, C28	Erie EDM 15 J
21-2509	Silver Mica	300V	5	33	1	C7	Erie EDM 15 J
21-2513	Silver Mica	300V	5	47	2	C9, C11	Erie EDM 15 J
21-2521	Silver Mica	300V	5	100	1	C22	Erie EDM 15 J
21-2537	Silver Mica	300V	5	470	2	C17, C20	Erie EDM 15 J
21-2503	Silver Mica	300V	5	18	1	C25	Erie EDM 15 J
21-3523	Polystyrene	30V	10	2200	1	C19	Suflex HS7/C
	or						
21-3520	Polystyrene	30V	2½	2200			Suflex HS7/C
21-6000	Trimmer			10-40	1	C18	Steatite Ins 10S-Triko-06
	DIODES						
22-1002	Silicon				2	D1, D2	Hughes HS9006
	TRANSISTORS						
22-6001	Silicon npn				2	Q1, Q2	Texas D1559
22-6008	Silicon pnp				1	Q3	Motorala 2N3906
22-6009	Silicon npn				1	Q4	Motorola 2N4124
23-7018	Choke		10	47μH	2	L6, L8	Painton 58/10/0015/10
23-7027	Choke		10	0.22μH	1	L7	Cambion 2960/22/3

Part No.	Description	Rat.	Tol. %	Value	Qty.	Component References	Vendor
				SHIFT REGISTER ASSEMBLY NO.19-0006			
	RESISTORS						
20-0103	Composition	1/10W	10	10k	8	R2, R14, R23, R30, R37, R44, R50, R51	Erie 15
20-0183	Composition	1/10W	10	18k	5	R7, R18, R33, R40, R47	Erie 15
20-0222	Composition	1/10W	10	2.2k	6	R9, R19, R27, R34, R41, R48	Erie 15
20-0333	Composition	1/10W	10	33k	12	R1, R10, R13, R20, R22, R28, R29, R35, R36, R42, R43, R49	Erie 15
20-0472	Composition	1/10W	10	4.7k	6	R4, R15, R24, R31, R38, R45.	Erie 15
20-0822	Composition	1/10W	10	8.2k	6	R5, R16, R25, R32, R39, R46.	Erie 15
20-2100	Metal Oxide	$\frac{1}{4}$W	5	10	1	R11	Erie MO4
20-2221	Metal Oxide	$\frac{1}{4}$W	5	220	1	R12	Erie MO4
20-2331	Metal Oxide	$\frac{1}{4}$W	5	330	1	R21	Erie MO4
20-2681	Metal Oxide	$\frac{1}{4}$W	5	680	4	R3, R8, R17, R26	Erie MO4
20-0221	Composition	1/10W	10	220	1	R6	Erie 15
	CAPACITORS						
21-1545	Ceramic	18V	-25 +50	0.010µ	1	C2	Erie 831/T/18V
21-1547	Ceramic	18V	-25 +50	0.033µ	7	C1, C3, C4, C5, C6, C7, C8	Erie 831/T/18V
	DIODES						
22-0000	Germanium				20	D1 - D20 Incl.	Mullard OA47
	TRANSISTORS						
22-5000	Germanium pnp				12	Q1, Q3, Q6, Q8, Q10, Q11, Q12, Q14, Q15, Q17, Q18, Q20	Mullard GET 882
22-5001	Germanium pnp				8	Q2, Q4, Q5, Q7, Q9, Q13, Q16, Q19	Mullard ACY 20
22-6008	Silicon pnp				1	Q21	Motorola 2N2906
	or						
22-6010	Silicon pnp						Motorola 2N4126

SEQUENCE CONTROL ASSEMBLY NO. 19-0007

Part No.	Description	Rat.	Tol. %	Value	Qty.	Component References	Vendor
	RESISTORS						
20-0104	Composition	1/10W	10	100k	1	R55	Erie 15
20-0102	Composition	1/10W	10	1k	1	R39	Erie 15
20-0103	Composition	1/10W	10	10k	6	R1, R25, R26, R30, R38, R45	Erie 15
20-0123	Composition	1/10W	10	12k	2	R10, R50	Erie 15
20-0152	Composition	1/10W	10	1.5k	2	R16, R46	Erie 15
20-0153	Composition	1/10W	10	15k	1	R22	Erie 15
20-0183	Composition	1/10W	10	18k	1	R31	Erie 15
20-0222	Composition	1/10W	10	2.2k	4	R17, R19, R24, R27	Erie 15
20-0332	Composition	1/10W	10	3.3k	1	R14	Erie 15
20-0333	Composition	1/10W	10	33k	2	R29, R37	Erie 15
20-0331	Composition	1/10W	10	330	1	R18	Erie 15
20-0473	Composition	1/10W	10	47k	6	R13, R23, R28, R40, R44, R47.	Erie 15
20-0562	Composition	1/10W	10	5.6k	4	R21, R48, R49, R52	Erie 15
20-0563	Composition	1/10W	10	56k	3	R15, R20, R2,	Erie 15
20-0683	Composition	1/10W	10	68k	1	R53	Erie 15
20-0822	Composition	1/10W	10	8.2k	3	R34, R35, R41	Erie 15
20-2100	Metal Oxide	1/4W	5	10	1	R43	Erie MO4
20-2123	Metal Oxide	1/4W	5	12k	1	R12	Erie MO4
20-2152	Metal Oxide	1/4W	5	1.5k	1	R51	Erie MO4
20-2182	Metal Oxide	1/4W	5	1.8k	2	R6, R8	Erie MO4
20-2221	Metal Oxide	1/4W	5	220	1	R33	Erie MO4
20-2222	Metal Oxide	1/4W	5	2.2k	1	R4	Erie MO4
20-2471	Metal Oxide	1/4W	5	470	1	R5	Erie MO4
20-2681	Metal Oxide	1/4W	5	680	1	R32	Erie MO4
20-2682	Metal Oxide	1/4W	5	6.8k	2	R7, R9	Erie MO4
20-2822	Metal Oxide	1/4W	5	8.2k	1	R11	Erie MO4
20-3100	Metal Oxide	1/2W	5	10	1	R36	Erie MO5
20-3182	Metal Oxide	1/2W	5	1.8k	1	R54	Erie MO5
20-3471	Metal Oxide	1/2W	5	470	1	R42	Erie MO5
20-6511	Variable		10	2.2k	1	RV1	Plessey G Mark 5A
20-6512	Variable		20	4.7k	1	RV2	Plessey G Mark 5A

Part No.	Description	Rat.	Tol. %	Value	Qty	Component References	Vendor
	CAPACITORS						
21-0500	Electrolytic	25V	- 20 +100	10µ	1	C15	Dubilier BR 5367
21-0502	Electrolytic	25V	- 20 +100	50µ	1	C13	Dubilier BR 0358
21-1524	Ceramic	500V	10	220	2	C2, C7	Erie 831
21-1532	Ceramic	500V	10	1000	4	C9, C10, C11, C12	Erie 831
21-1545	Ceramic	18V	10	0.01µ	1	C5	Erie 831/T/18V
21-1547	Ceramic	18V	10	0.033µ	2	C18, C20	Erie 831/T/18V
21-4506	Polyester	100V	10	0.1µ	6	C8, C14, C16, C17, C19, C21	Waycom MKS
21-4510	Polyester	100V	10	0.47µ	1	C4	Waycom MKS
21-4512	Polyester	100V	10	1µ	1	C3	Waycom MKS
21-4505	Polyester	250V	10	0.068µ	1	C1	Waycom MKS
21-1530	Ceramic	500V	10	680	1	C6	Erie 831
	DIODES						
22-0000	Germanium				7	D2 - D8 Incl	Mullard OA47
22-1000	Silicon				1	D1	Hughes HS1010
22-1001	Silicon				1	D9	Hughes HS7062
	TRANSISTORS						
22-5000	Germanium				12	Q1, Q2, Q3, Q5, Q6, Q7, Q8, Q9, Q10, Q12, Q13, Q15	Mullard GET 882
22-5001	Germanium				3	Q11, Q14, Q17	Mullard ACY 20
22-6000	Silicon				1	Q4	Fairchild U2956/5
22-5003	Silicon				1	Q16	Mullard 2N1309
	INTER-CONNECTING ASSEMBLY NO. 19-0008						
	RESISTORS						
20-0221	Composition	1/10W	10	220	1	R1	Erie 15
20-0103	Composition	1/10W	10	10k	5	R2, R3, R4, R5, R6	
23-5010	Edge Connector 20 Way				1		Pressac 60/052/FR
23-5011	Edge Connector 13 Way				2		Pressac 60/053/FR

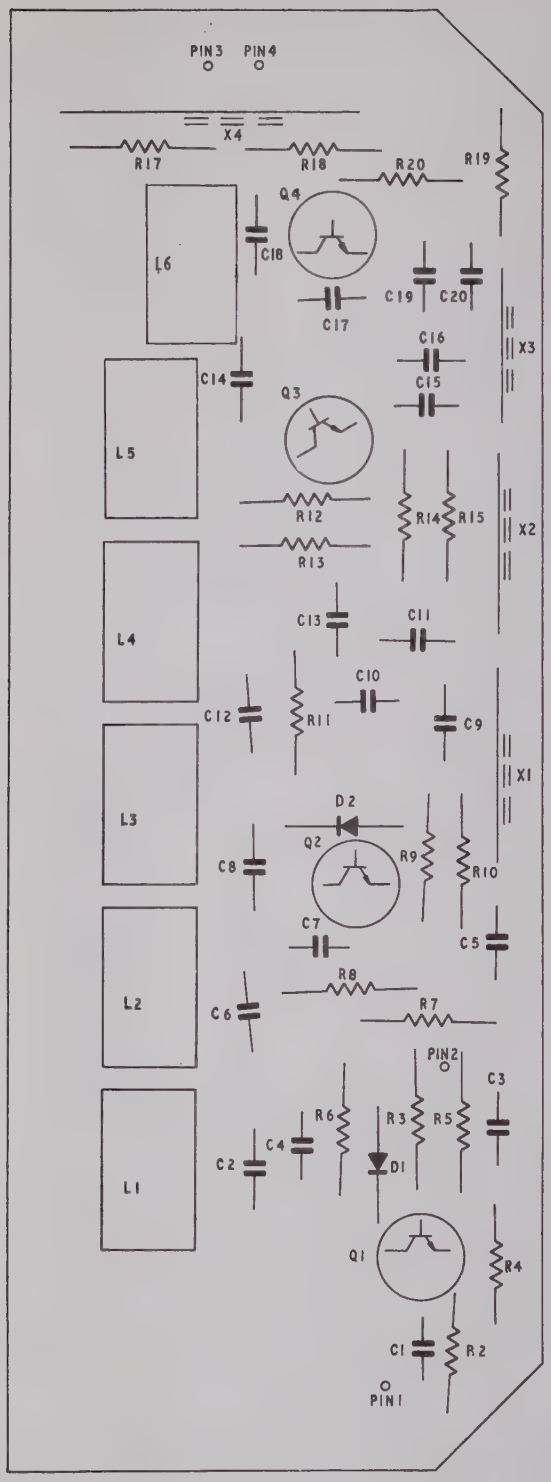
Part No.	Description	Rat.	Tol. %	Value	Qty	Component References	Vendor
				ATTENUATOR PRINTED CIRCUIT BOARD NO.190061			
	RESISTORS						
20-3221	Metal Oxide	½W	10	220	1	R2.....	Erie MO5
20-3680	Metal Oxide	½W	10	68	2	R1, R3.....	Erie MO5
20-0181	Composition	1/10W	10	180	1	R4.....	Erie 15
	CAPACITORS						
21-2583	Silver Mica Button	500V	10	3000	1		Erie 651-004
21-1500	Ceramic			2.2	1	C2.....	Erie 831
21-1505	Ceramic			5.6	1	C3.....	Erie 831
				RECTIFIER POWER ASSEMBLY - MODEL 1 NO.19-0088			
	RESISTORS						
20-0103	Composition	1/10W	10	10k	2	R1, R2.....	Erie 15
	CAPACITORS						
21-0509	Electrolytic	25V		250µ	1	C1.....	Waycom A6-1
	or						
21-0513	Electrolytic	25V		200µ			Waycom A6-1
22-1622	Rectifier Silicon PIV	100V			4	D1, D2, D3, D4.....	A.E.I. MS2H
	or						
22-1624	Rectifier Silicon PIV	300V					A.E.I. MS5H
	or						
22-1602	Rectifier Silicon PIV	100V					Motorola 1N4002
22-1602	Rectifier Silicon PIV	100V			8	D5 - D12 Incl.....	Motorola 1N4002
	or						
22-1603	Rectifier Silicon PIV	200V					Motorola 1N4003
	or						
22-1604	Rectifier Silicon PIV	400V					Motorola 1N4004

STABILISED POWER ASSEMBLY NO.19-0090

Part No.	Description	Rat.	Tol. %	Value	Qty	Component References	Vendor
	RESISTORS						
20-2101	Metal Oxide	¼W	5	100	1	R3	Erie MO4
20-2122	Metal Oxide	¼W	5	1.2k	2	R7, R8	Erie MO4
20-2271	Metal Oxide	¼W	5	270	2	R12, R15	Erie MO4
20-2272	Metal Oxide	¼W	5	2.7k	1	R10	Erie MC4
20-2332	Metal Oxide	¼W	5	3.3k	1	R11	Erie MO4
20-2471	Metal Oxide	¼W	5	470	2	R14, R17	Erie MO4
20-2681	Metal Oxide	¼W	5	680	1	R9	Erie MO4
20-3181	Metal Oxide	½W	5	180	1	R4	Erie MO5
20-6522	Variable Composition			500	2	R13, R16	Plessey MP (Dealer)
	CAPACITORS						
21-0512	Electrolytic	25V		100µ	2	C6, C7	Sprague 36D/362/G040/AB2C
	or						
21-0507	Electrolytic	15V		120µ			T.C.C. CE9H
21-1545	Ceramic	18V		0.01µ	2	C4, C5	Erie 831/T/18V
	DIODES						
22-1810	Silicon Zener		5	6.2V	2	D13, D14	Mullard BZY 88-C6V2
22-1807	Silicon Zener		5	4.7V	1	D15	Mullard BZY 88-C4V7
	TRANSISTORS						
22-6009	Silicon npn				4	Q2, Q4, Q6, Q7	Motorola 2N4124
	or						
22-6007	Silicon npn						Motorola 2N3904
22-6010	Silicon pnp				1	Q5	Motorola 2N4126
	or						
22-6008	Silicon pnp						Motorola 2N3906

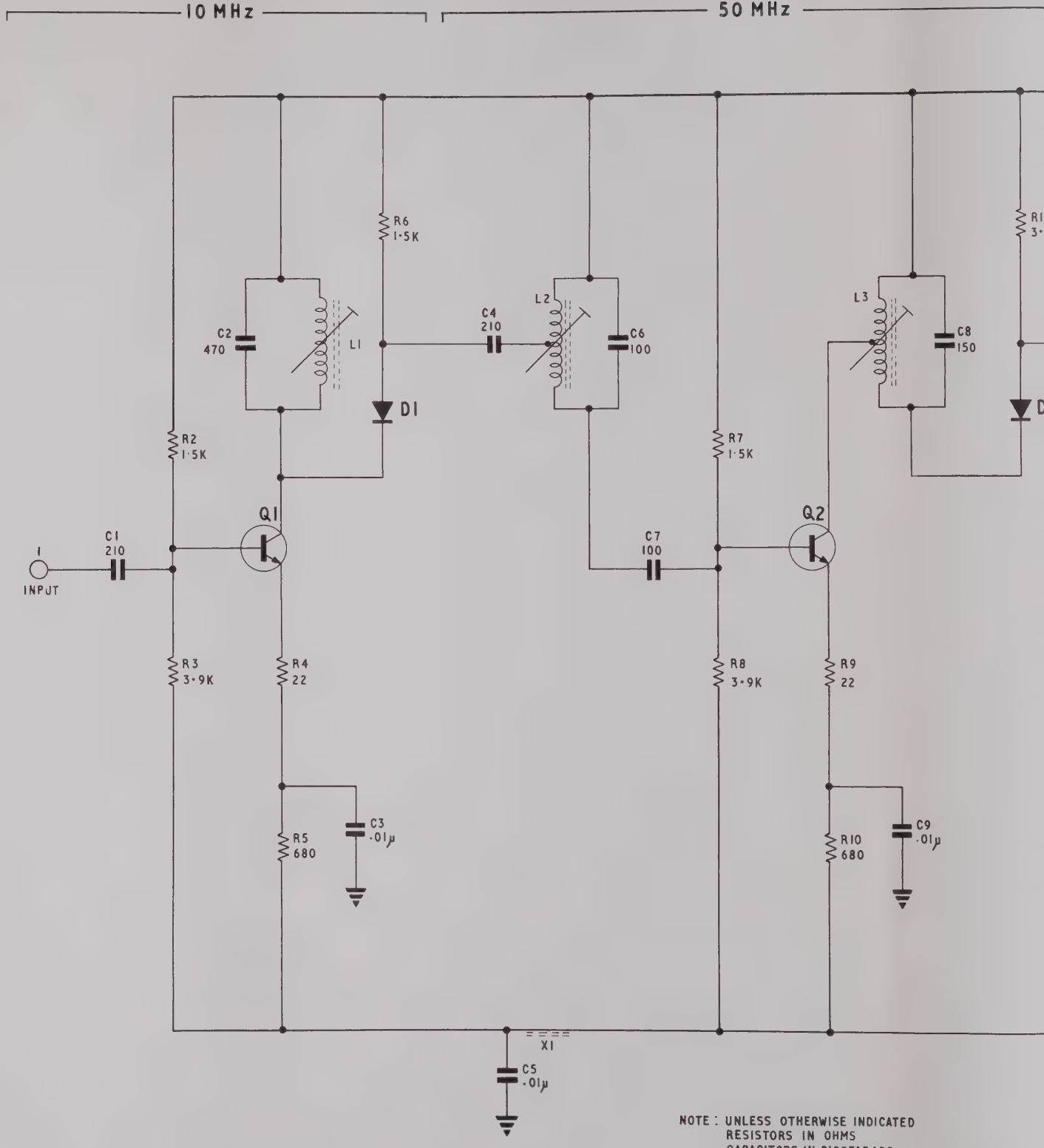
Part No.	Description	Rat.	Tol. %	Value	Qty	Component References	Vendor
				EXTERNAL STANDARD ASSEMBLY NO.19-0160			
17-3024	Coil Assembly				1	L1	Racal Instr.
	RESISTORS						
20-0102	Composition	1/10W	±10	1k	1	R5	Erie 15
20-0103	Composition	1/10W	±10	10k	1	R1	Erie 15
20-0222	Composition	1/10W	±10	2.2k	1	R3	Erie 15
20-0272	Composition	1/10W	±10	2.7k	1	R4	Erie 15
20-2562	Metal Oxide	¼W	± 5	5.6k	1	R6	Erie MO4
20-3102	Metal Oxide	½W	± 5	1k	1	R2	Erie MO5
	CAPACITORS						
21-1520	Ceramic			100	1	C1	Erie 831
21-1532	Ceramic			1000	1	C4	Erie 831
21-1591	Ceramic	100V		0.01µ	2	C2, C3	Erie 801
21-2537	Silver Mica			470	1	C5	Dubilier D10
	DIODES						
22-1006	Diode				1	D1	Hughes HS9010
	TRANSISTORS						
22-6001	Silicon npn				2	Q1, Q2	Texas D1559
	RESISTORS						
20-2820	Metal Oxide	¼W	5	82	1	R7	
20-2101 *	Metal Oxide	¼W	5	100			
20-2680 *	Metal Oxide	¼W	5	68			
20-2121 *	Metal Oxide	¼W	5	120			
20-2560 *	Metal Oxide	¼W	5	56			

* Alternative select-on-test values for R7

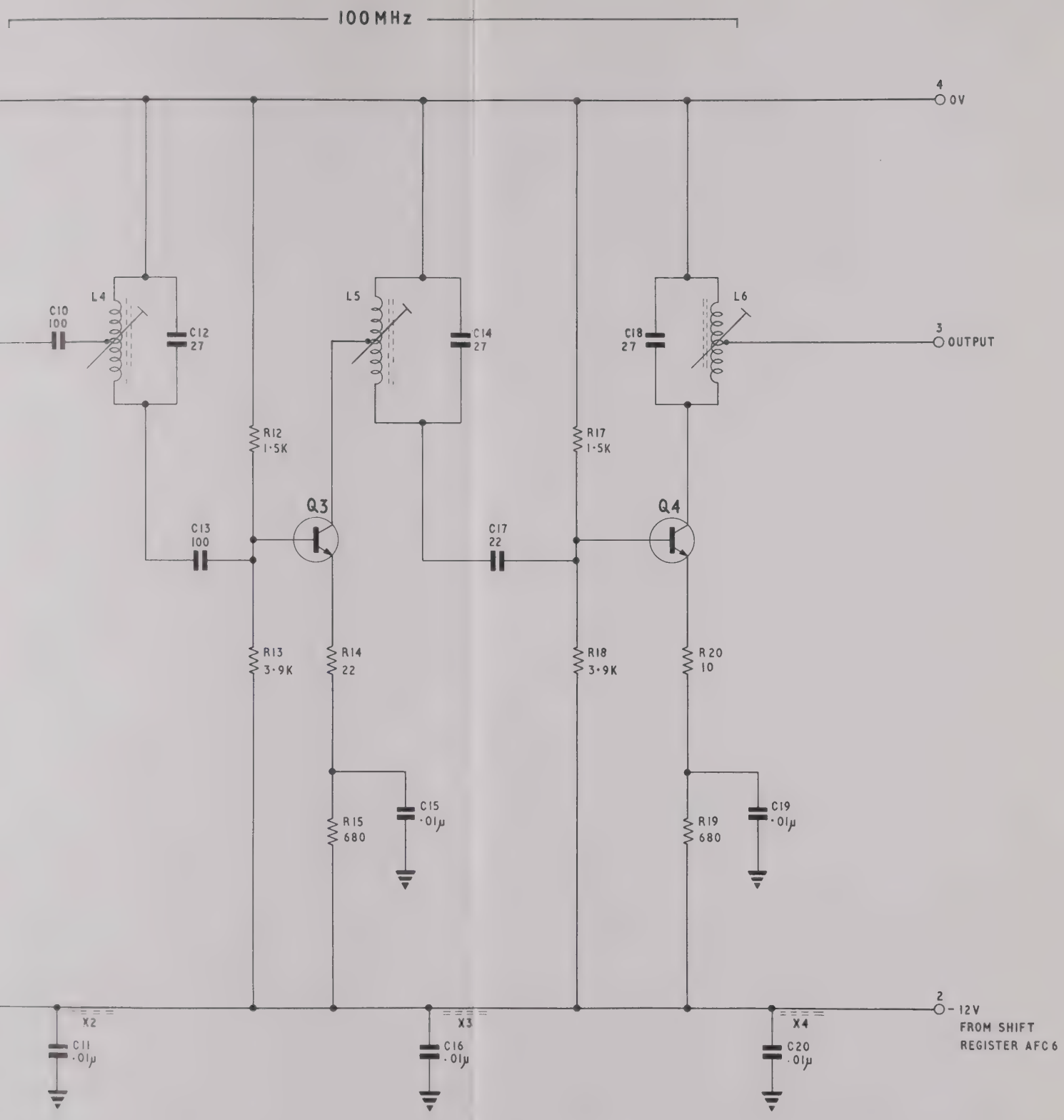


ISSUE	
1	6-9-67

FREQ. MULTIPLIER ASSY. | 19-0001 SHT. 1 OF 2



NOTE : UNLESS OTHERWISE INDICATED
RESISTORS IN OHMS
CAPACITORS IN PICOFARADS



ISSUE		
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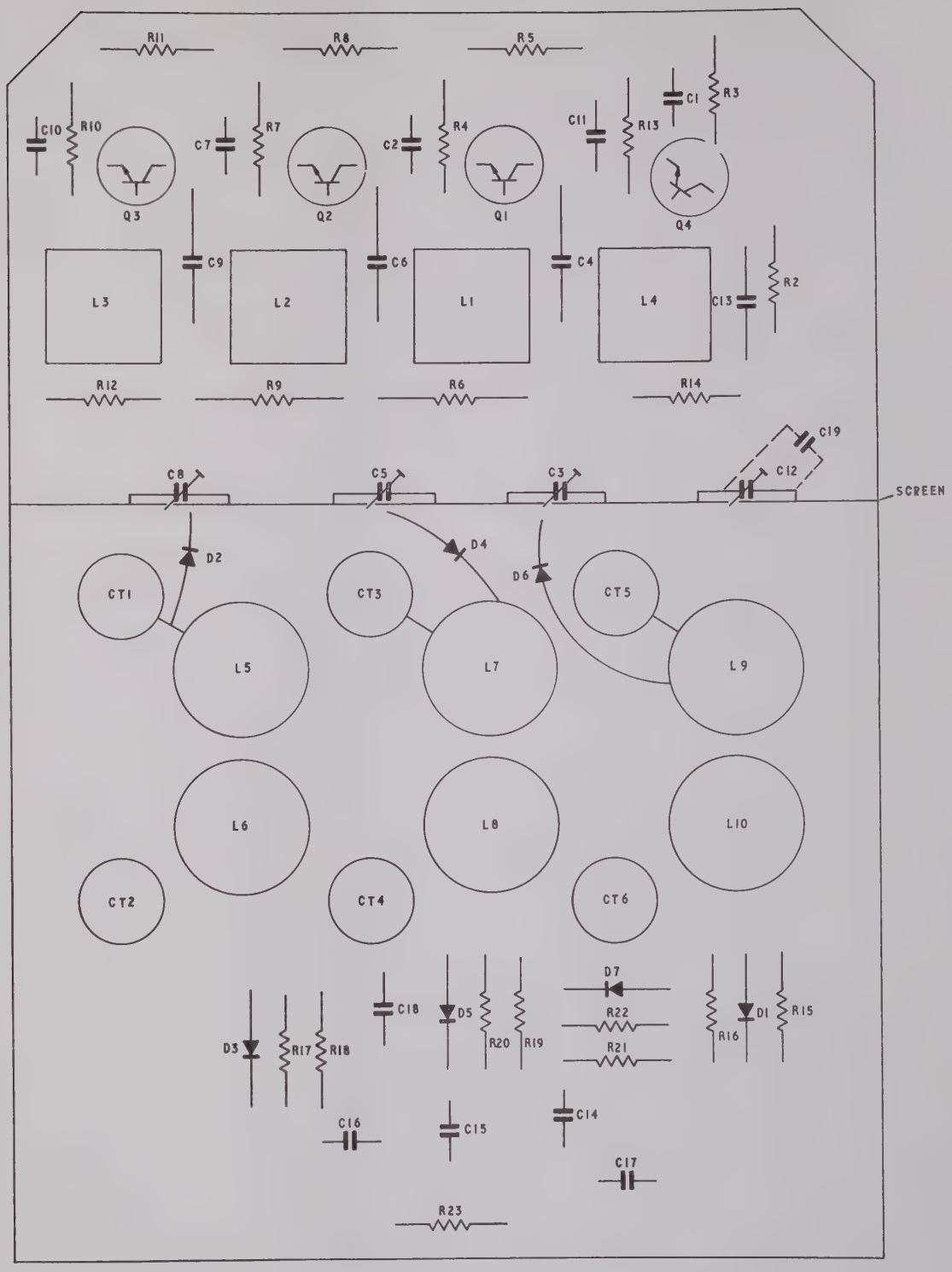
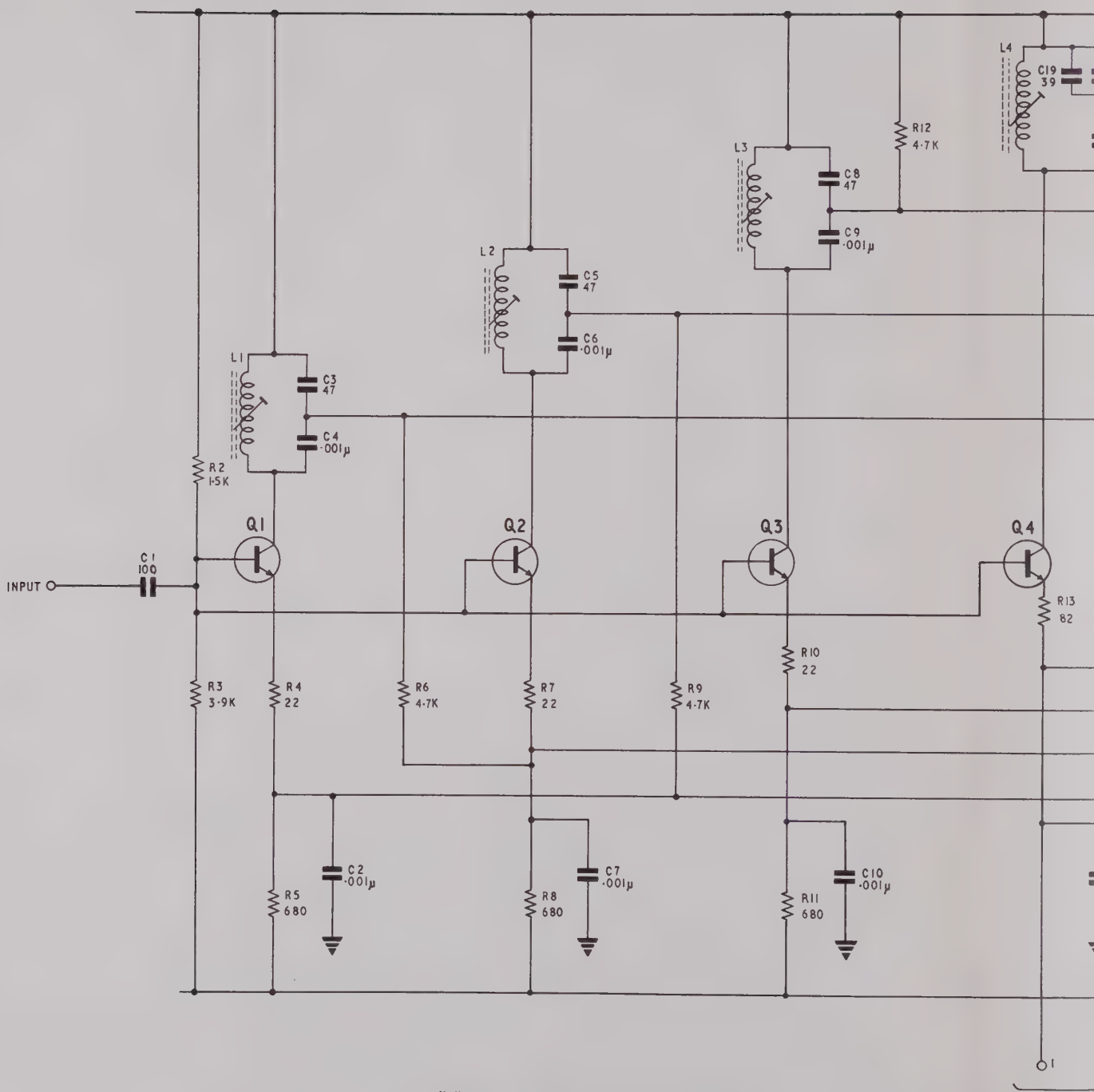
3	23 8 67	CN10520

FREQUENCY MULTIPLIER ASSY	19-0001	SHT. 2 OF 2.

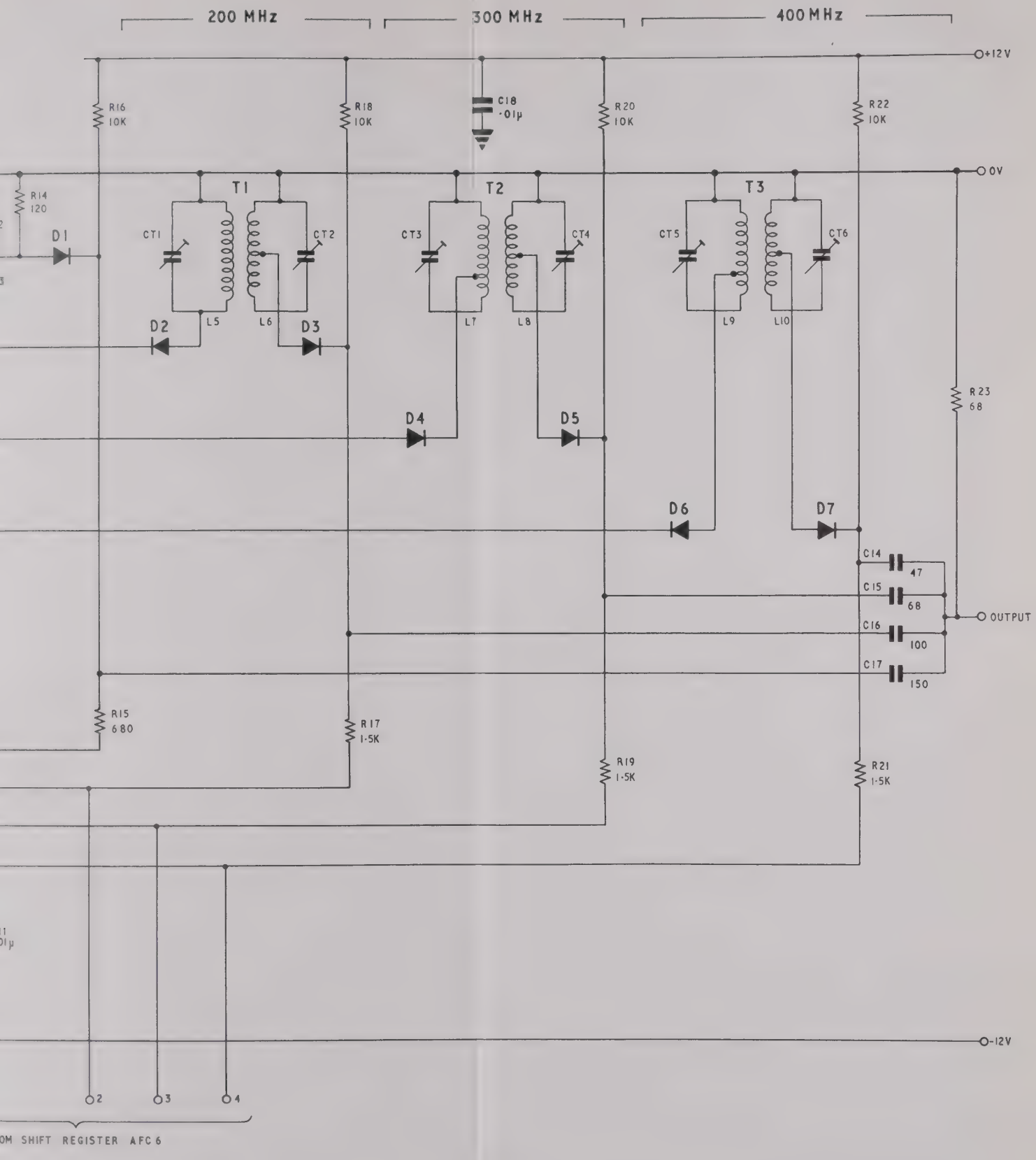


ISSUE	1	7.9.67		
HARMONIC GENERATOR ASSEMBLY			19-0002	SHT 1 OF 2

100 MHz



NOTE:
1. UNLESS OTHERWISE INDICATED
RESISTORS IN OHMS. CAPACITORS IN PICOFARADS.



ISSUE		
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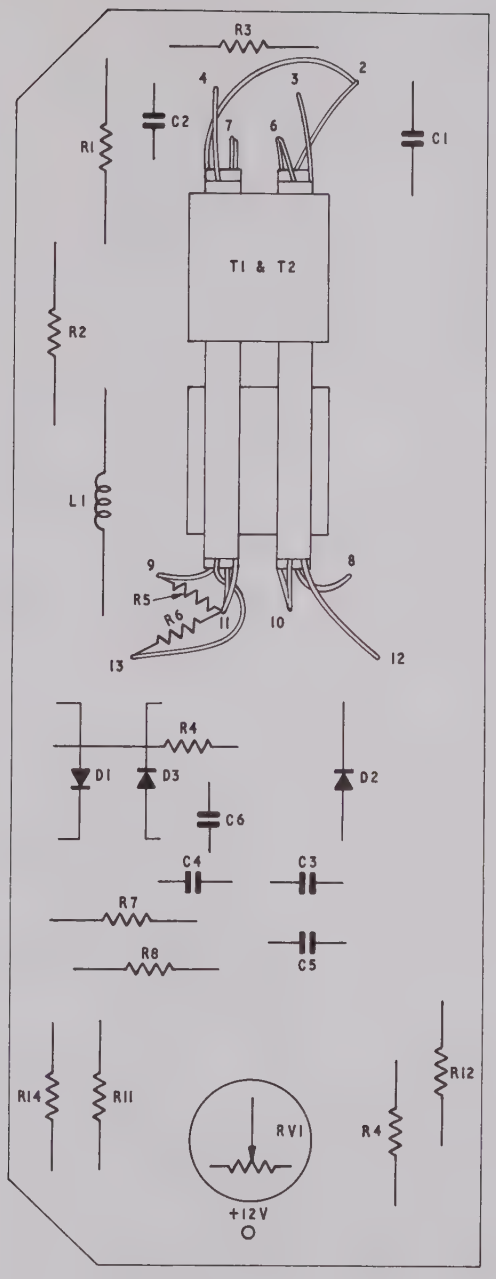
3	5·9·67	CN10520

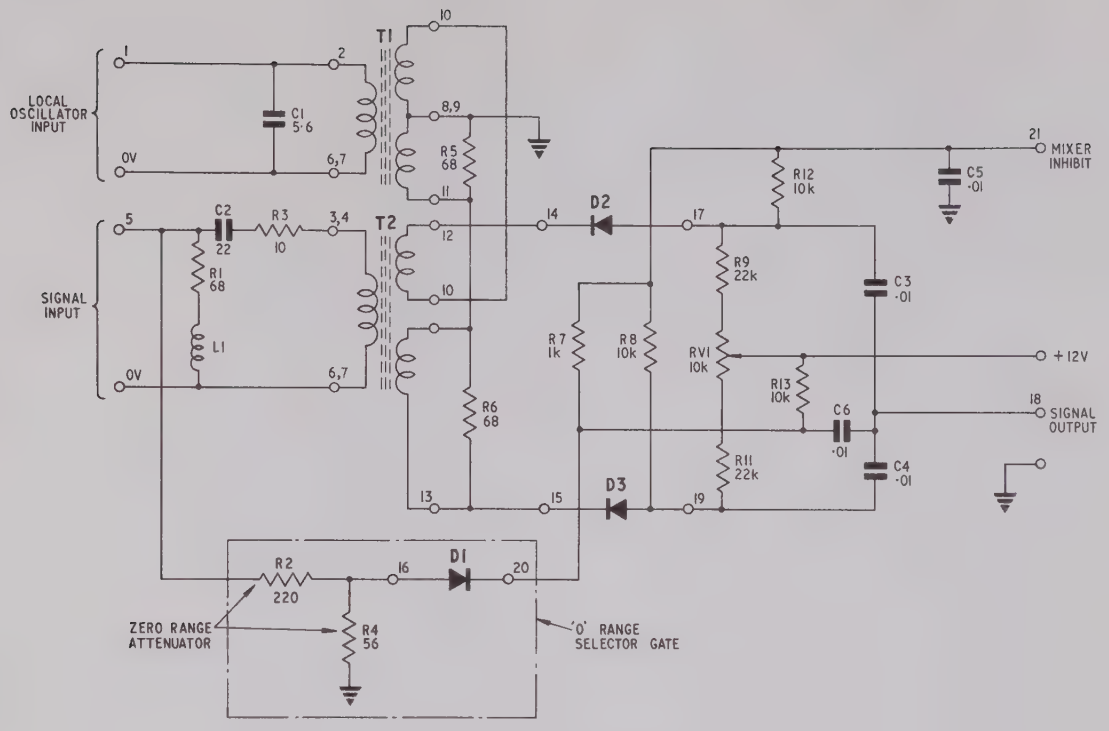
H.G.A. HARMONIC GENERATOR ASSY. 19-0002 SHT.2 OF 2



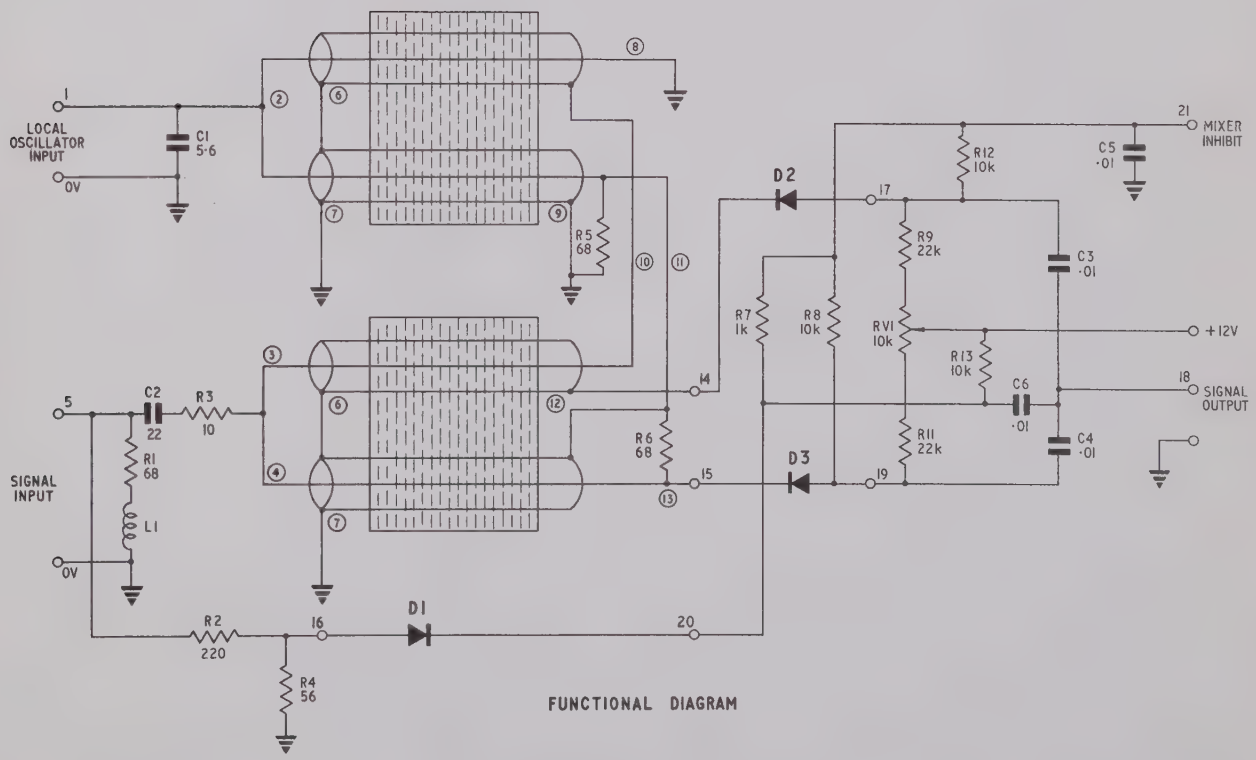
ISSUE	
2	15·9·67 CN10526

BALANCED MIXER ASSY.

19-0003 SHT. 1 OF 2.



THEORETICAL DIAGRAM

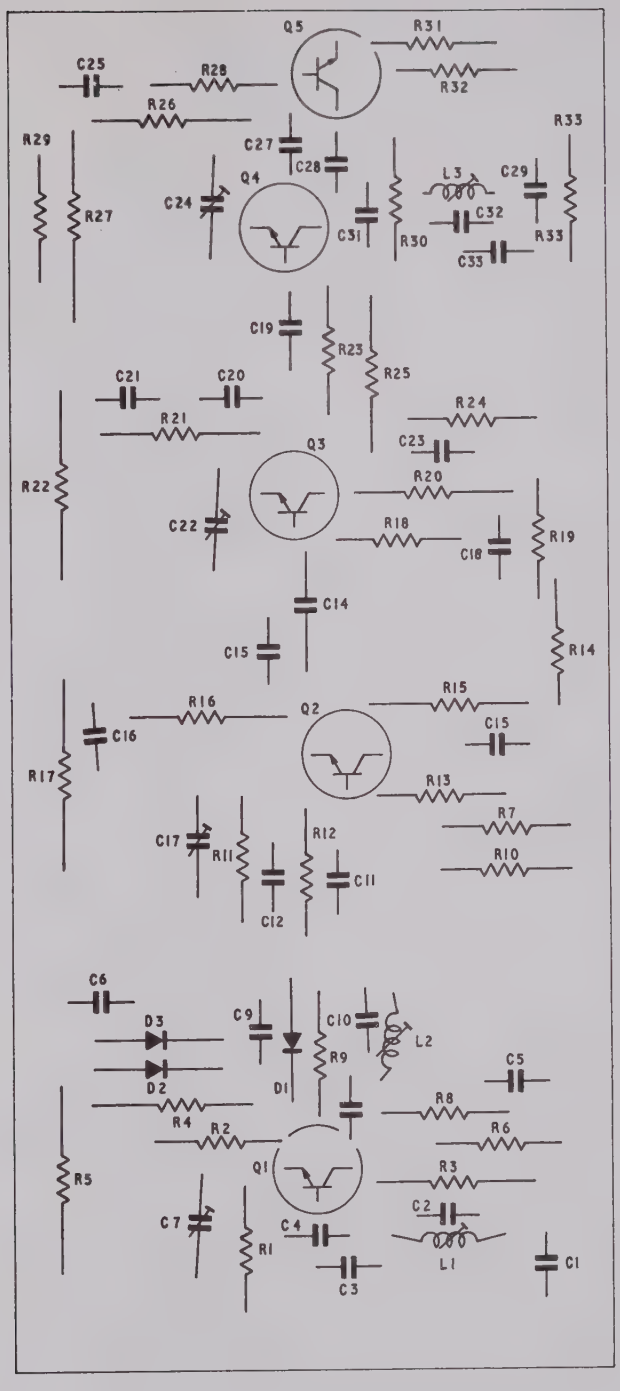


FUNCTIONAL DIAGRAM

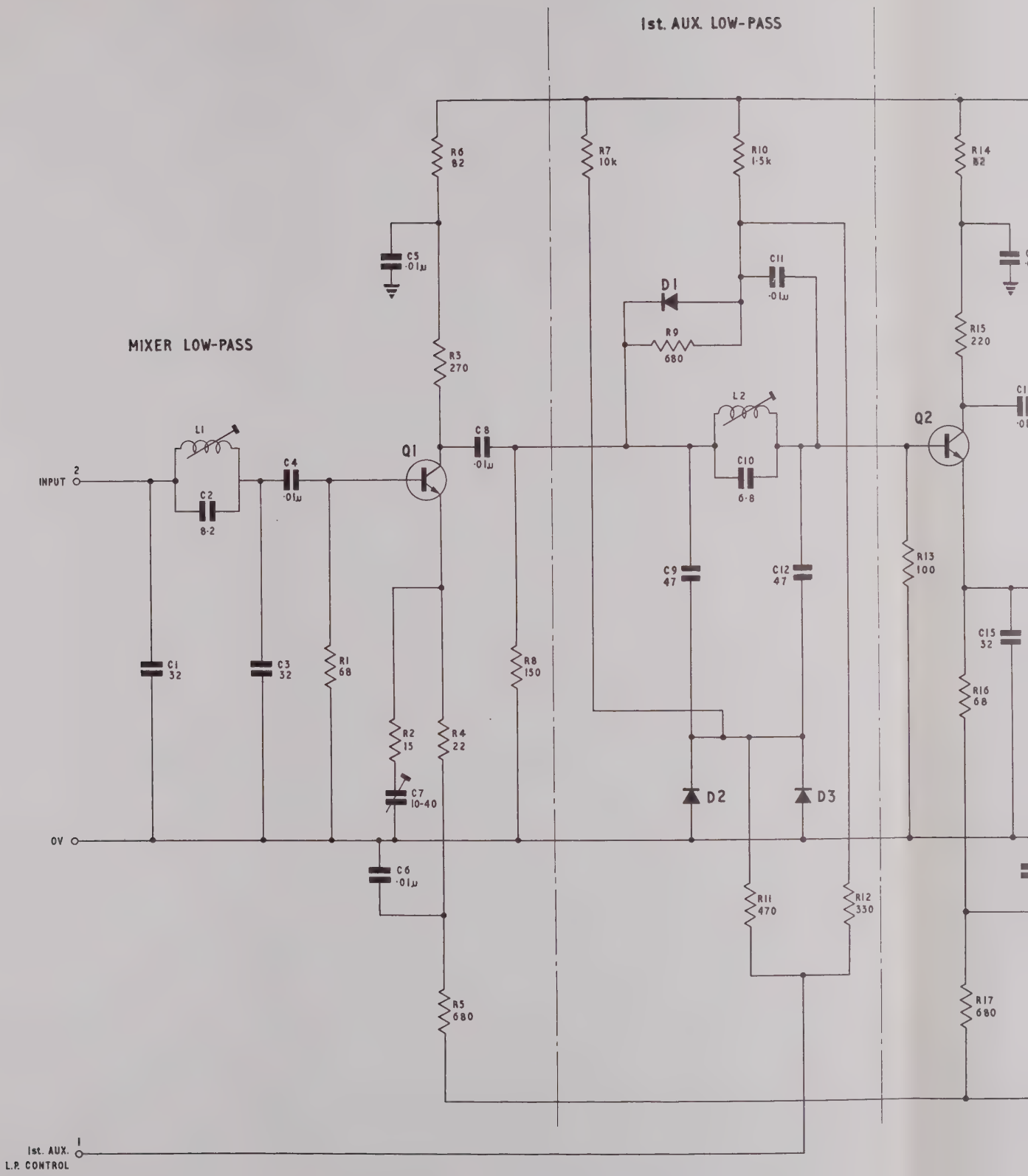
NOTE.
UNLESS OTHERWISE STATED:
RESISTORS IN OHMS.
CAPACITORS IN PICOFARADS.

ISSUE		
2.	Re-drawn	CN. 10516
3.	15-9-67	CN. 10526

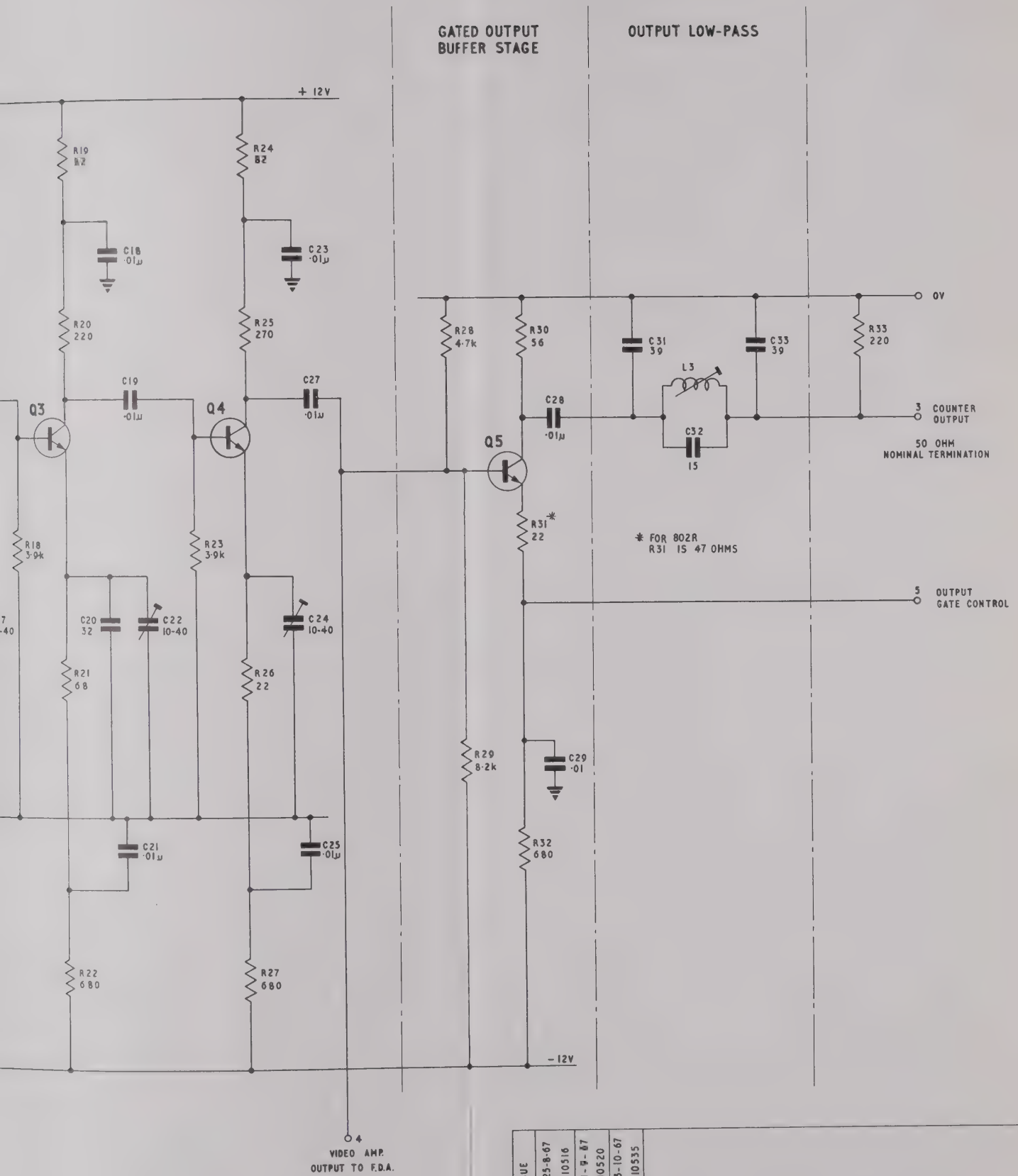
BALANCED MIXER ASSEMBLY	19-0003	SHT. 2 OF 2



ISSUE		
	VIDEO AMPLIFIER ASSY.	19-0004 SHT. 1 OF 2



NOTE.
UNLESS OTHERWISE STATED:
RESISTORS IN OHMS.
CAPACITORS IN PICOFARADS.

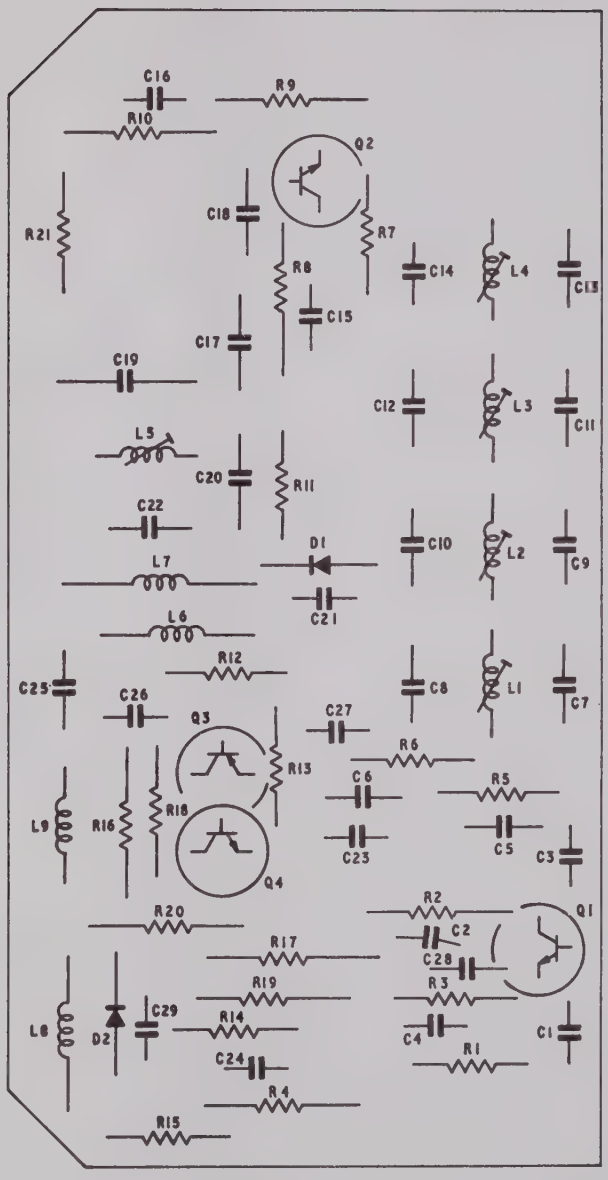


ISSUE						
2	25-8-67	3	11-9-67	4	13-10-67	
CN 10516		CN. 10520		CN. 10535		

VIDEO AMPLIFIER ASSEMBLY

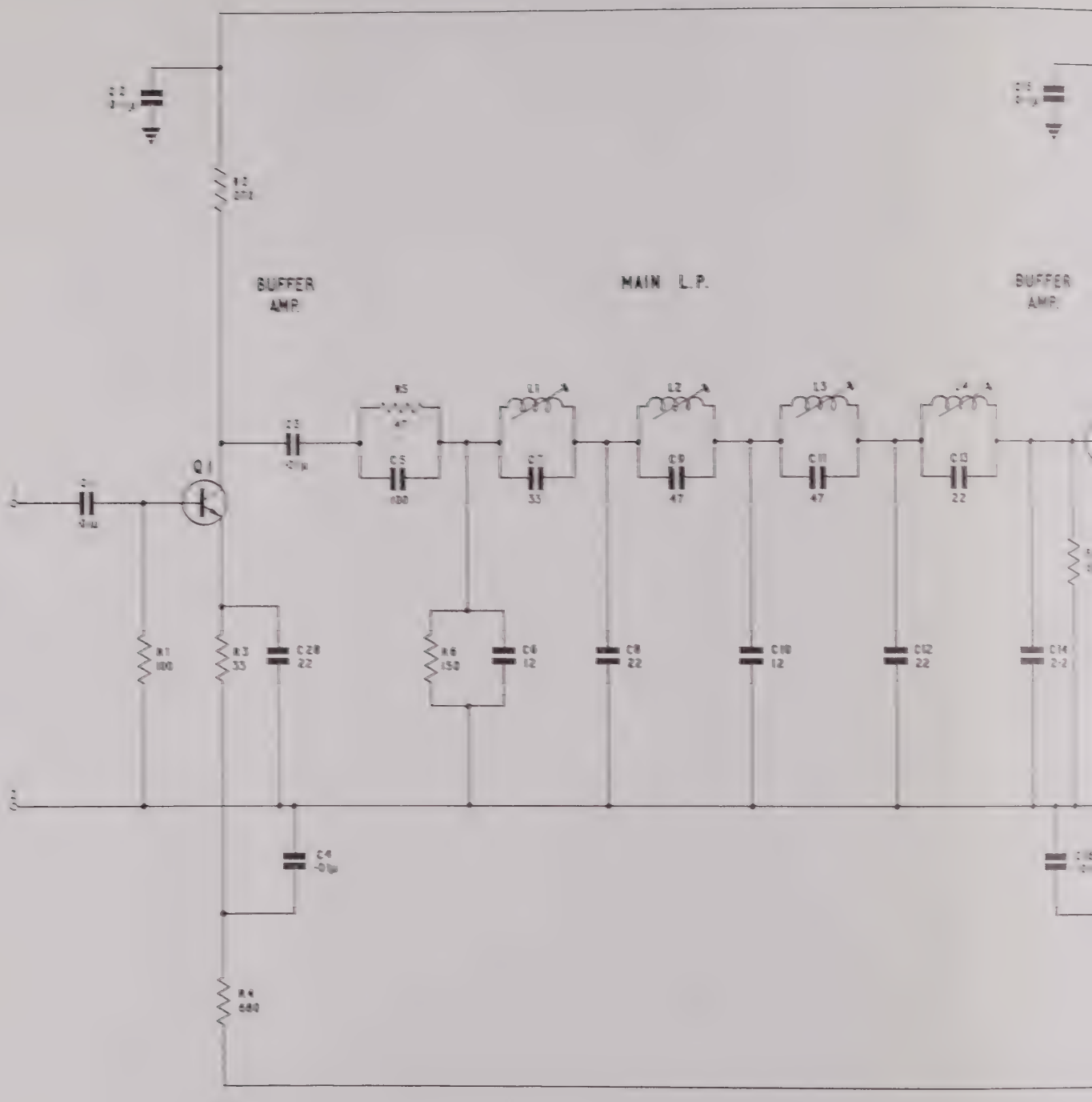
19-0004

SHT. 2 OF 2

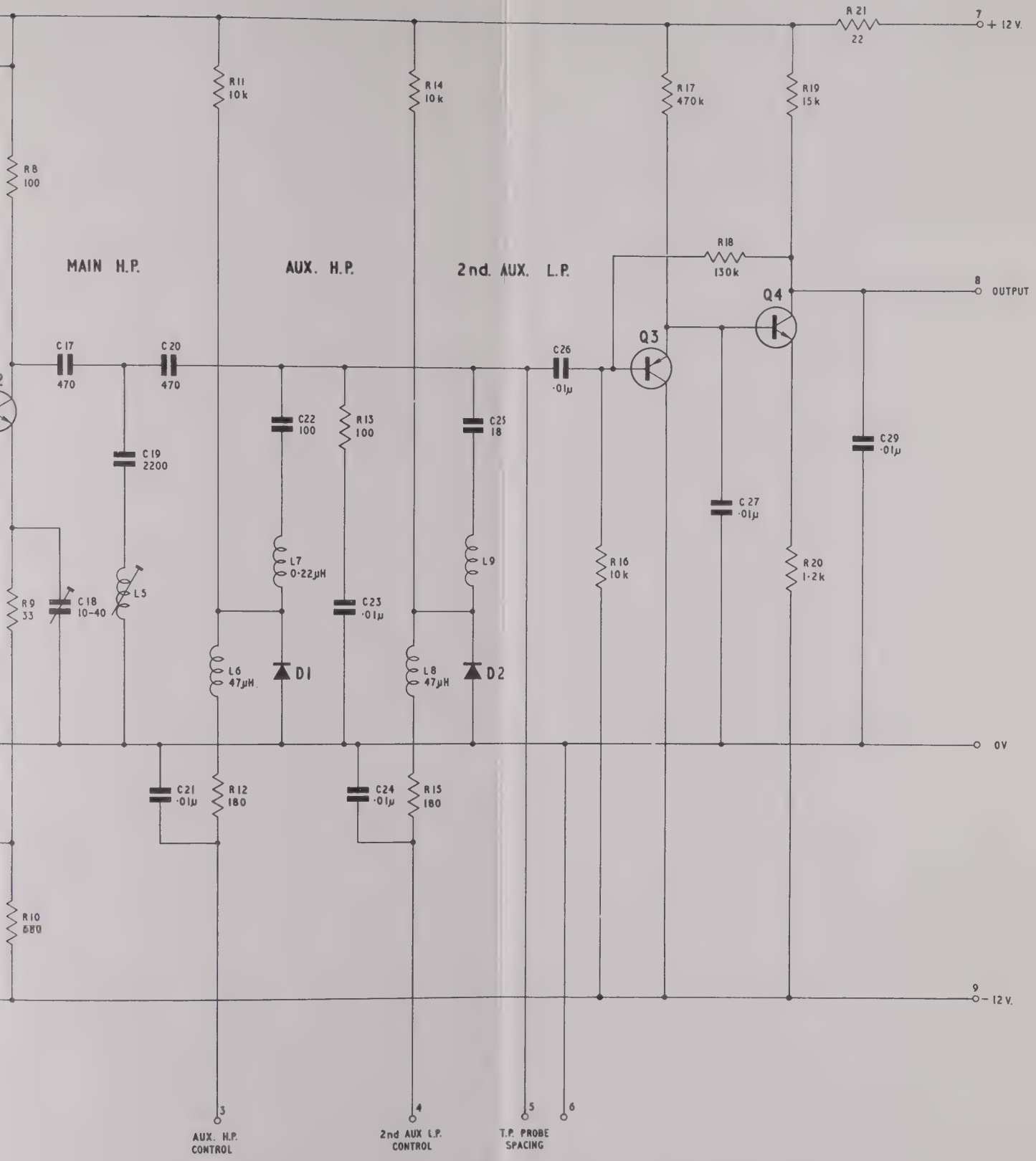


ISSUE	
1 25-8-67	

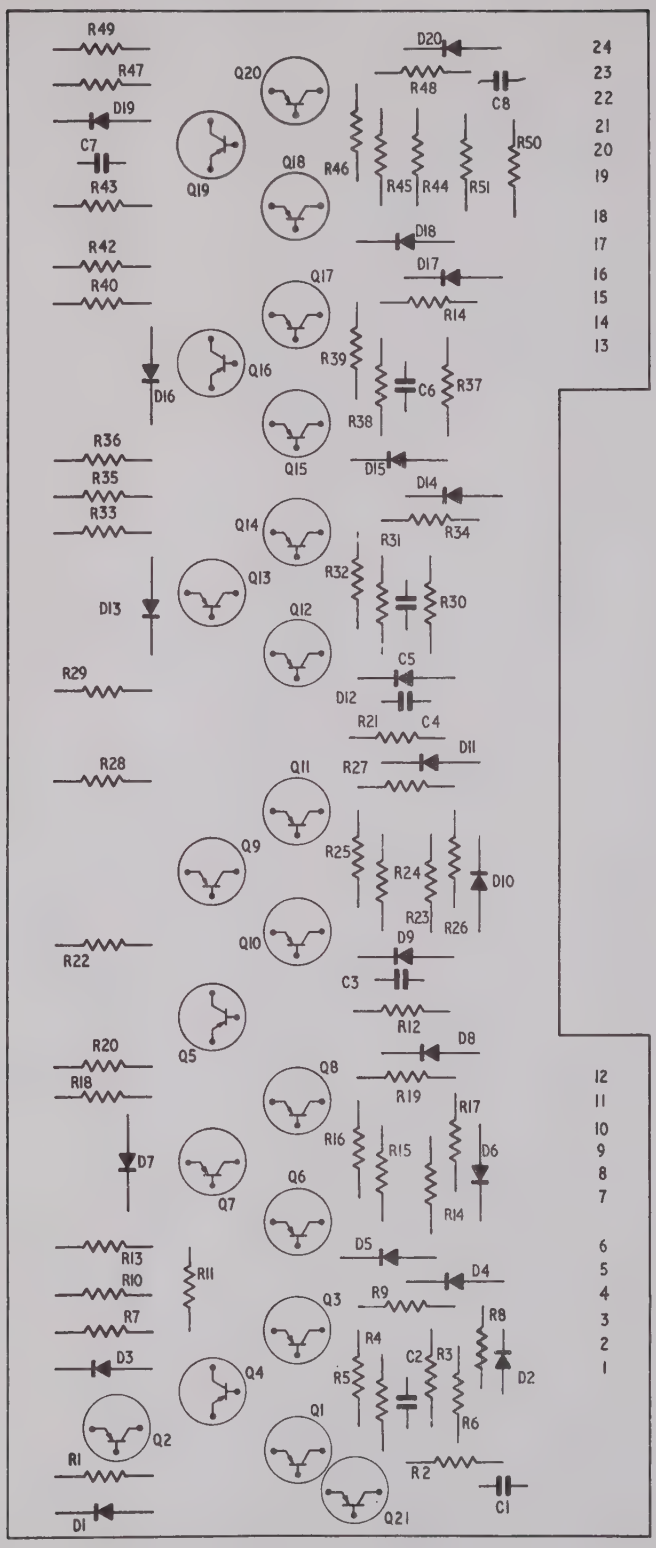
FILTER DETECTOR ASSY. 19-0005 SHT. 1 OF 2



NOTE
UNLESS OTHERWISE STATED
RESISTORS IN OHMS.
CAPACITORS IN PICOFARADS.

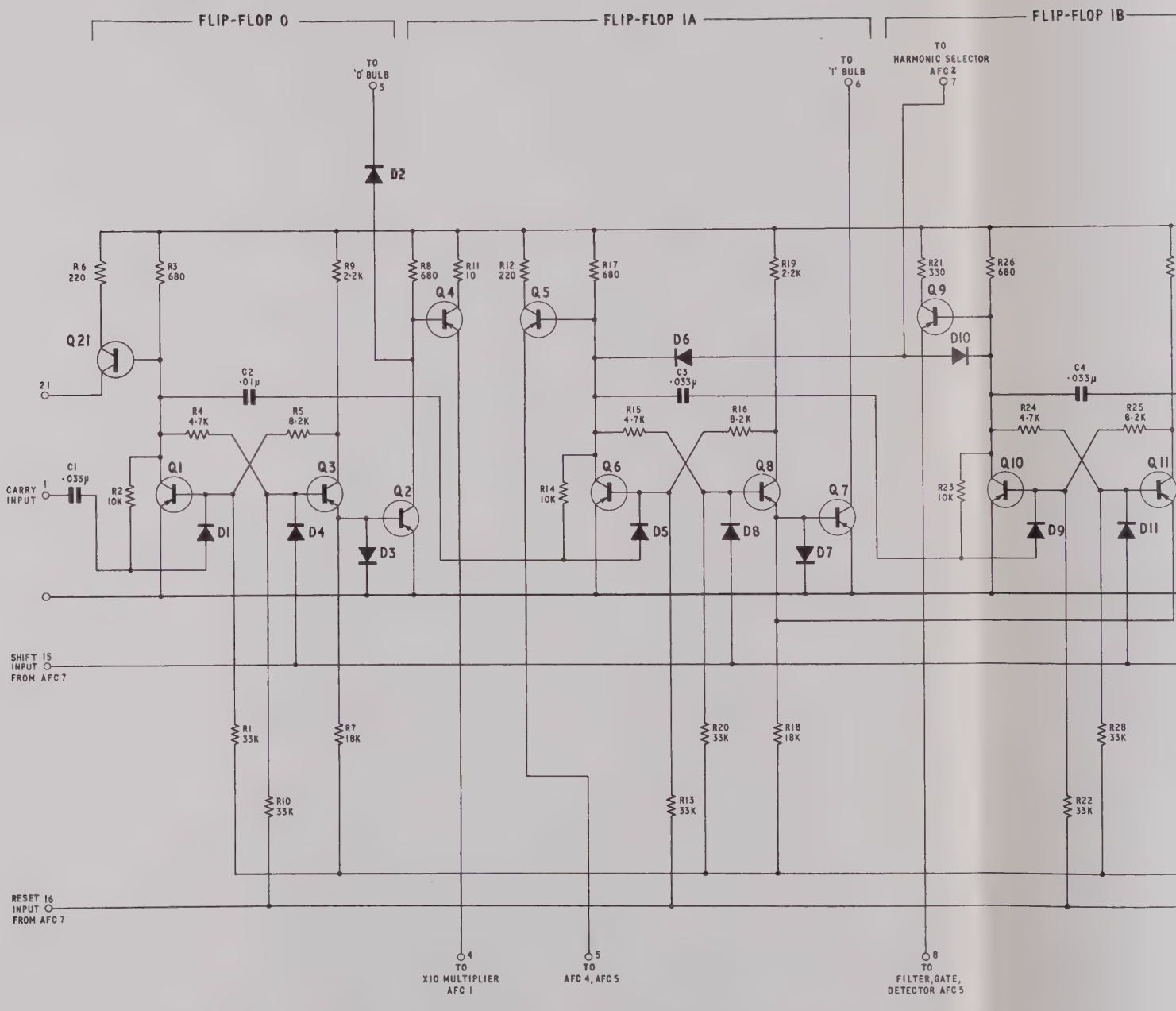


ISSUE	2	25-8-67	C.N. 10510	
FILTER DETECTOR ASSY.			19-0005	SHT. 2 OF 2

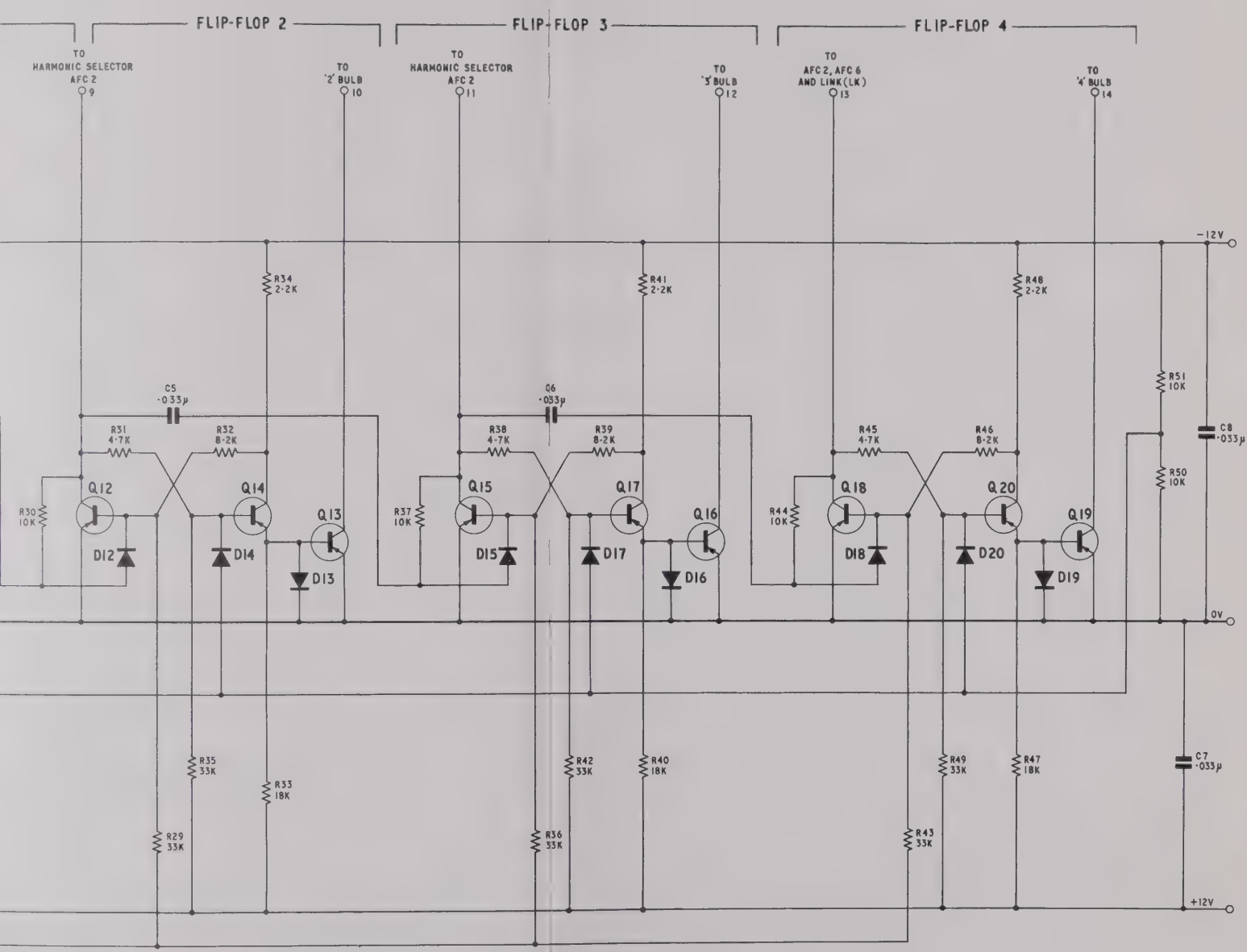


ISSUE	
3	14-9-67
	CN. 10520

SHIFT REGISTER ASSY. 19-0006 SHT. 1 OF 2

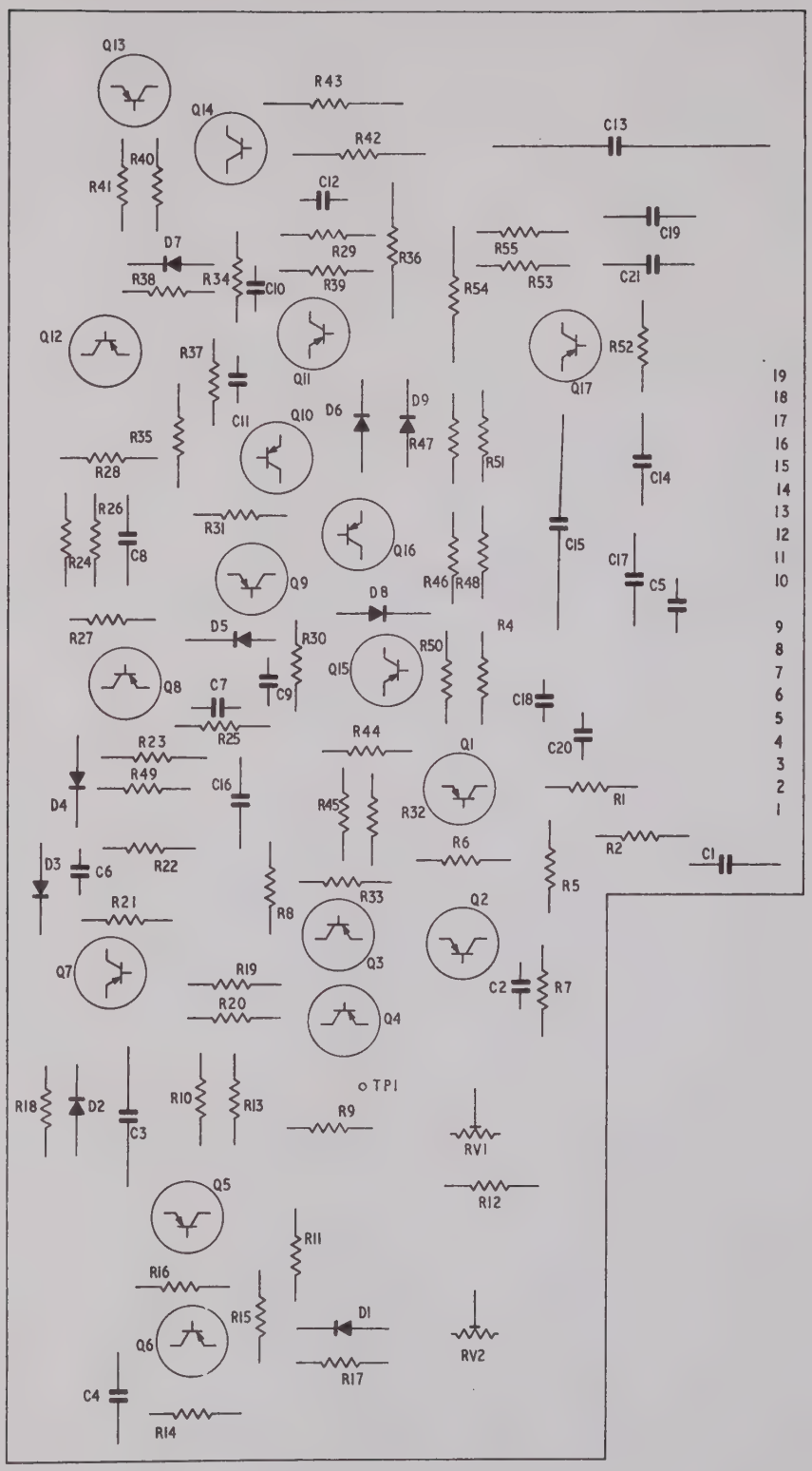


NOTE:
UNLESS OTHERWISE INDICATED;
RESISTORS IN OHMS. CAPACITORS IN PICOFARADS.



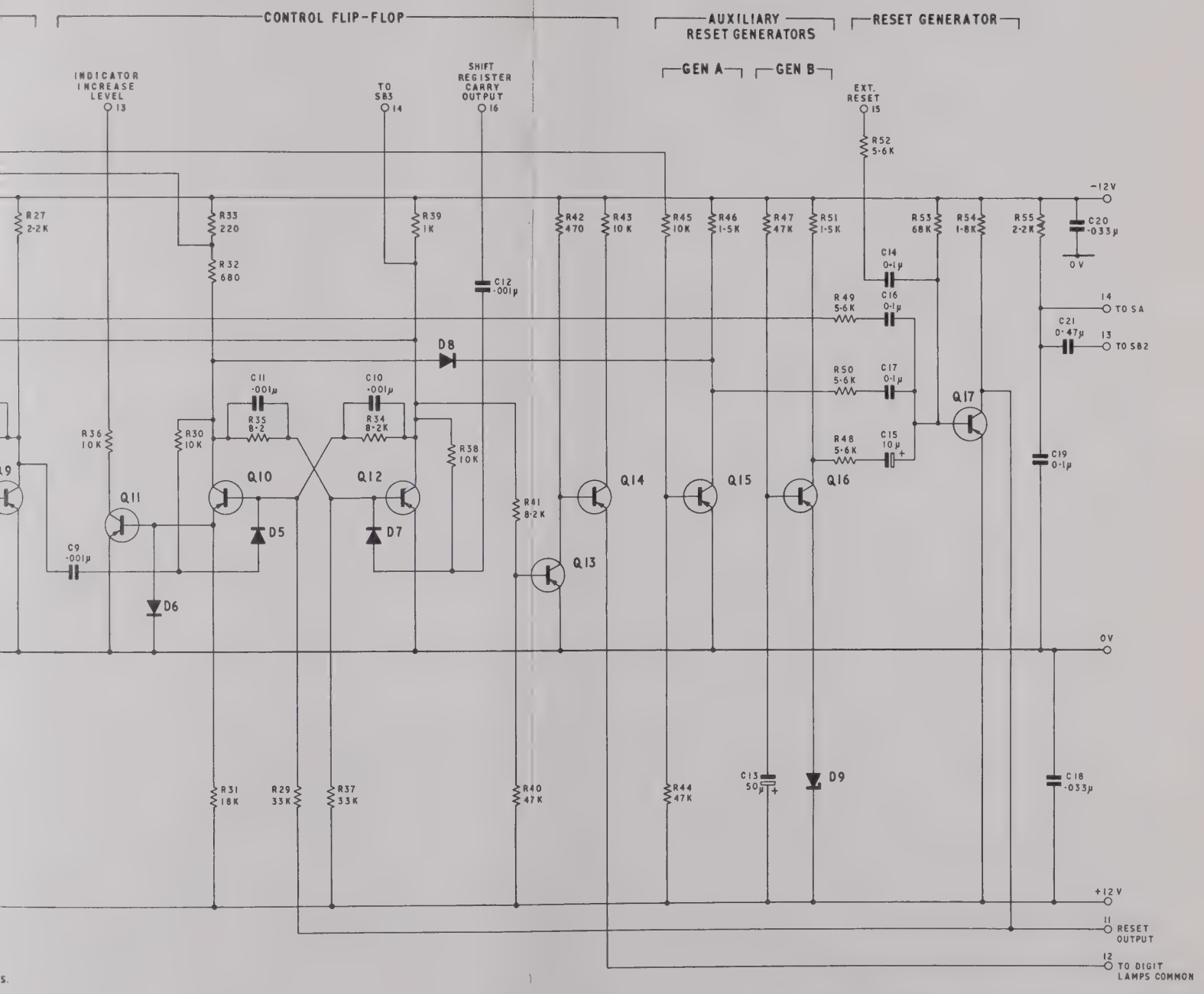
ISSUE		
2	10·3·67	CN10369
3	23·8·67	CN10520

SHIFT REGISTER ASSY. 19-0006 SHT. 2 OF 2



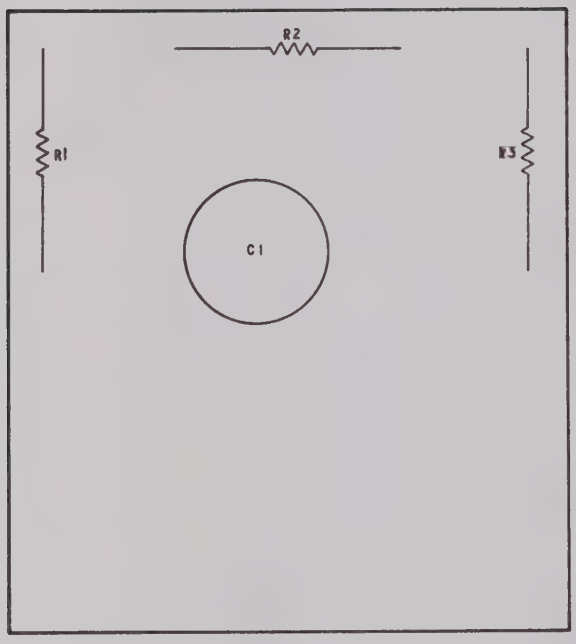
ISSUE	
1	

SEQUENCE CONTROL ASSY. 19-0007 SHT. 1 OF 2



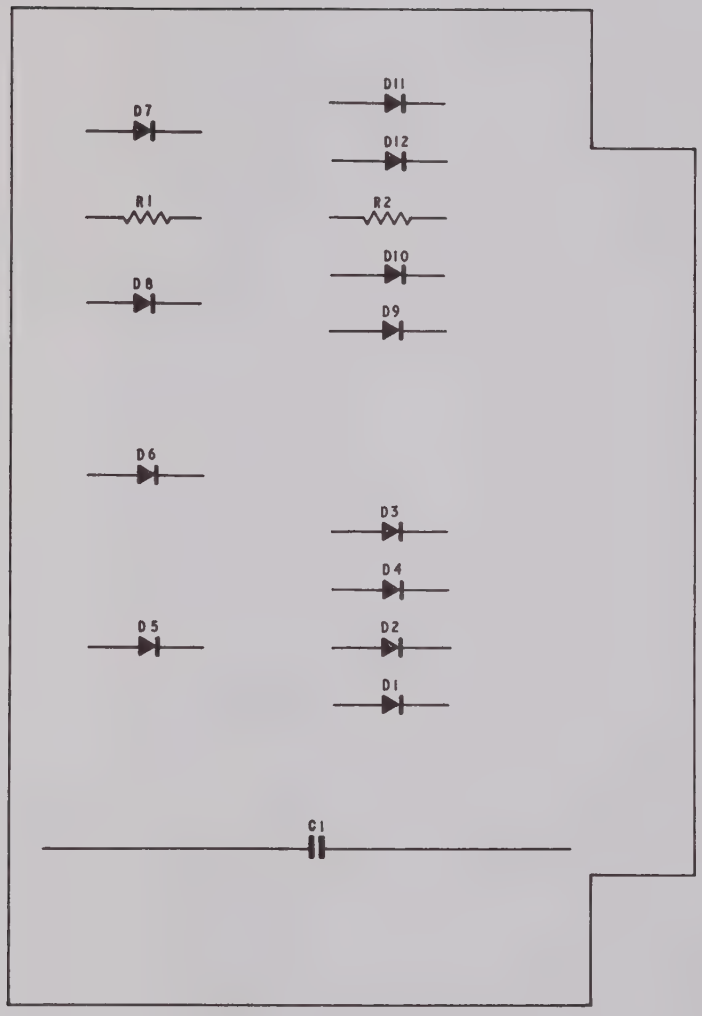
ISSUE		
2	21 12 66	CN 10280
3	20 2 67	CN 10352
4	13 3 67	CN 10369
5	23 8 67	CN 10520
6	27 11 67	CN 10582

SEQUENCE CONTROL ASSY. 19-0007 SHT. 2 OF 2

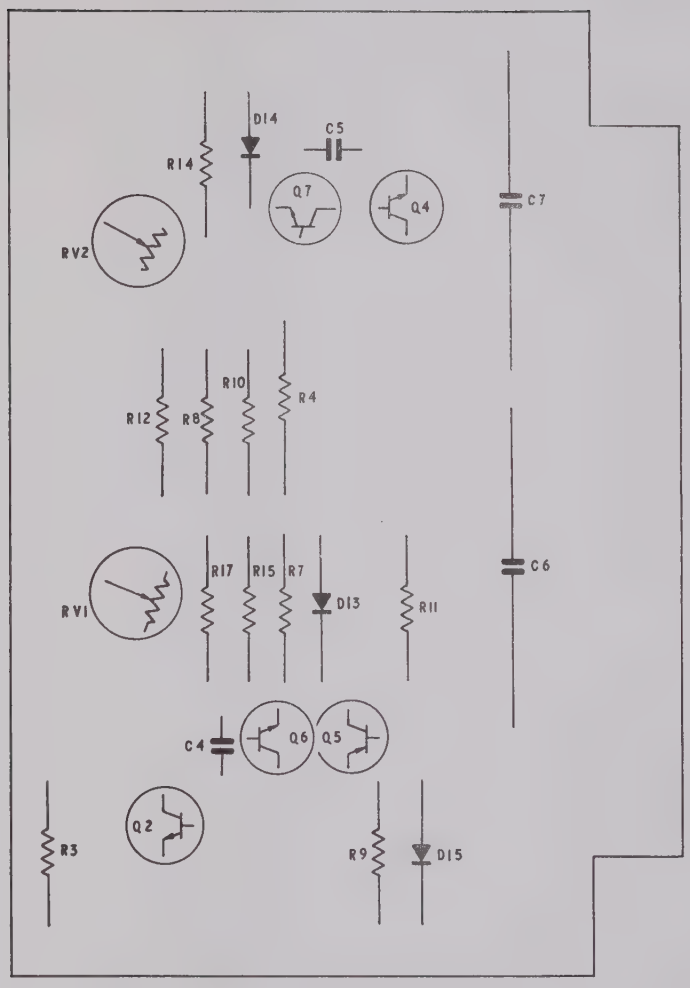


ISSUE	
1	16-3-67

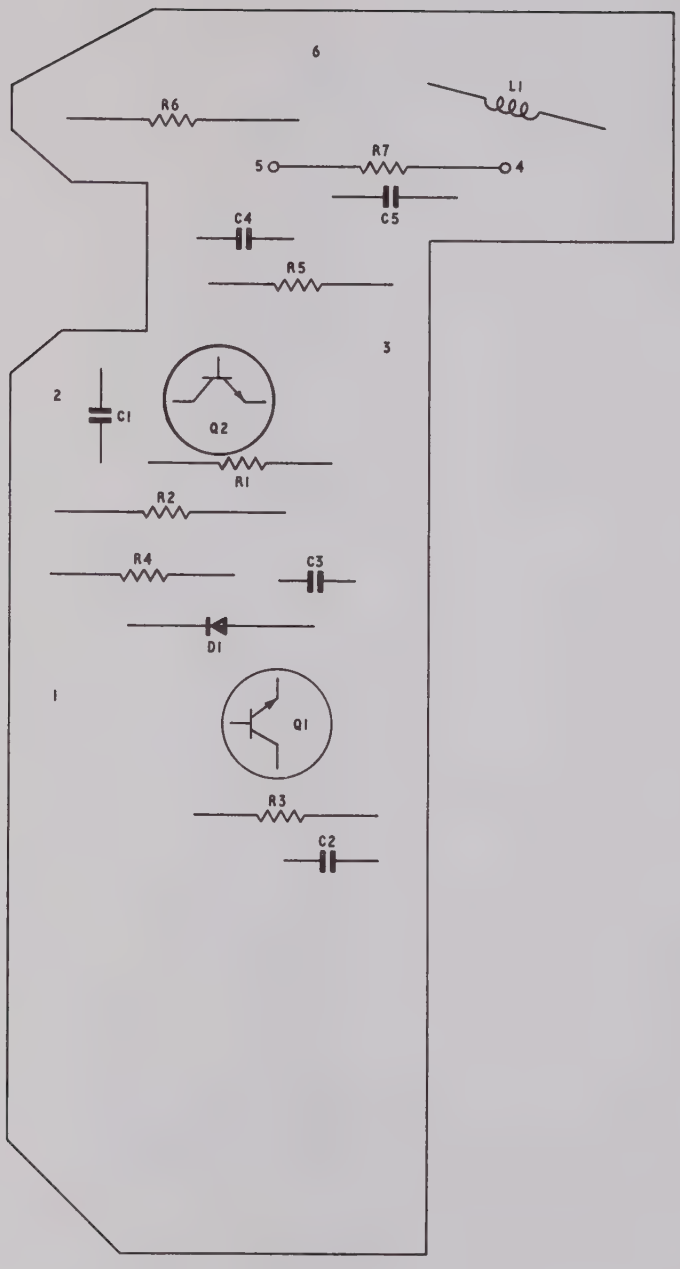
ATTENUATOR P.C.B. ASSY | 19-0061



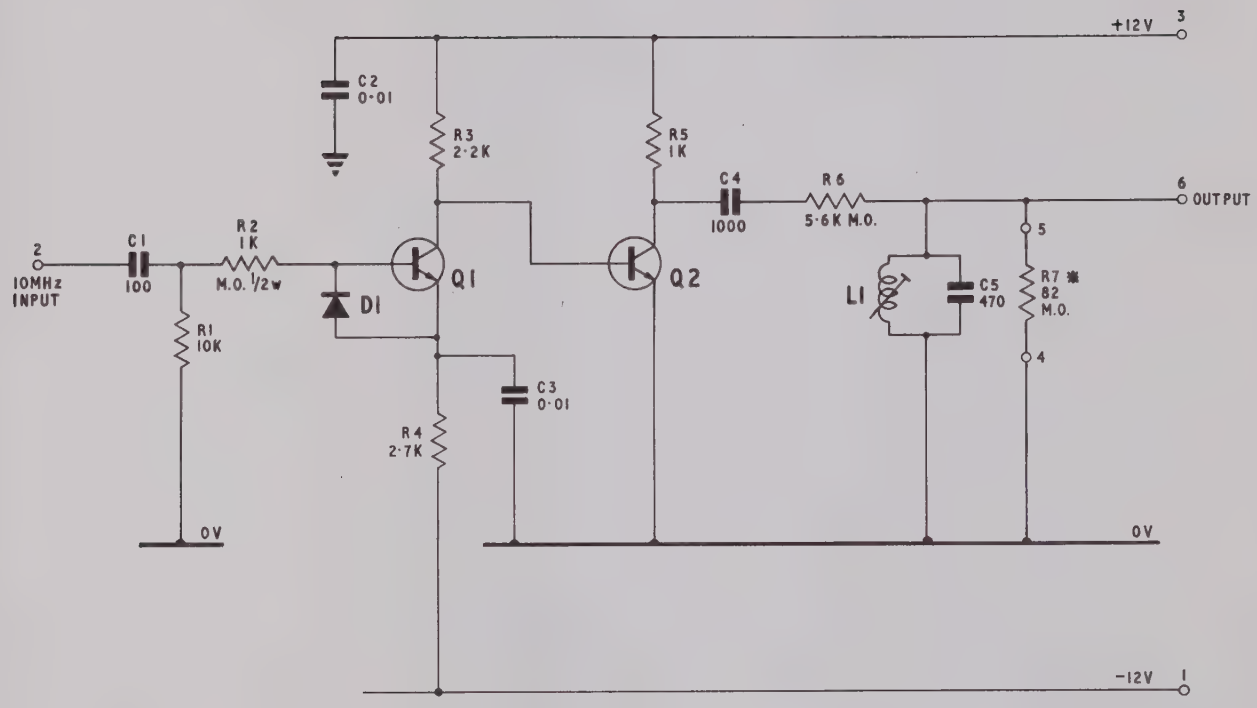
ISSUE	1	15·1·67	
RECTIFIER POWER ASSEMBLY MODEL 1			19-0088



ISSUE	2 · 5 · 67 CN10388	
STABILISED POWER ASSEMBLY		19-0090



ISSUE	
EXTERNAL STANDARD AMP.	19-0160 SHT 1 OF 2



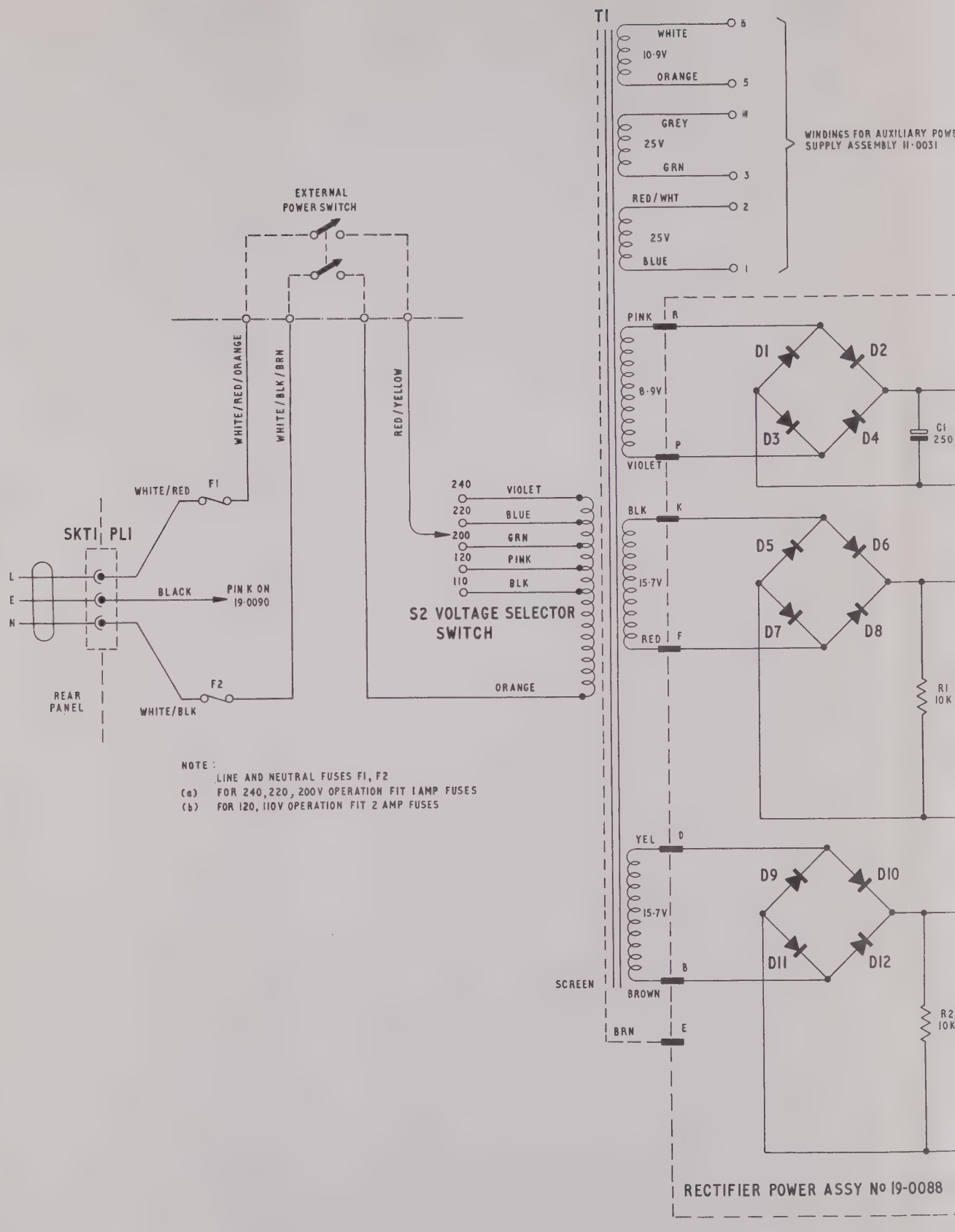
NOTES:

1. UNLESS OTHERWISE INDICATED:
   RESISTORS IN OHMS. CAPACITORS IN PICOFARADS.

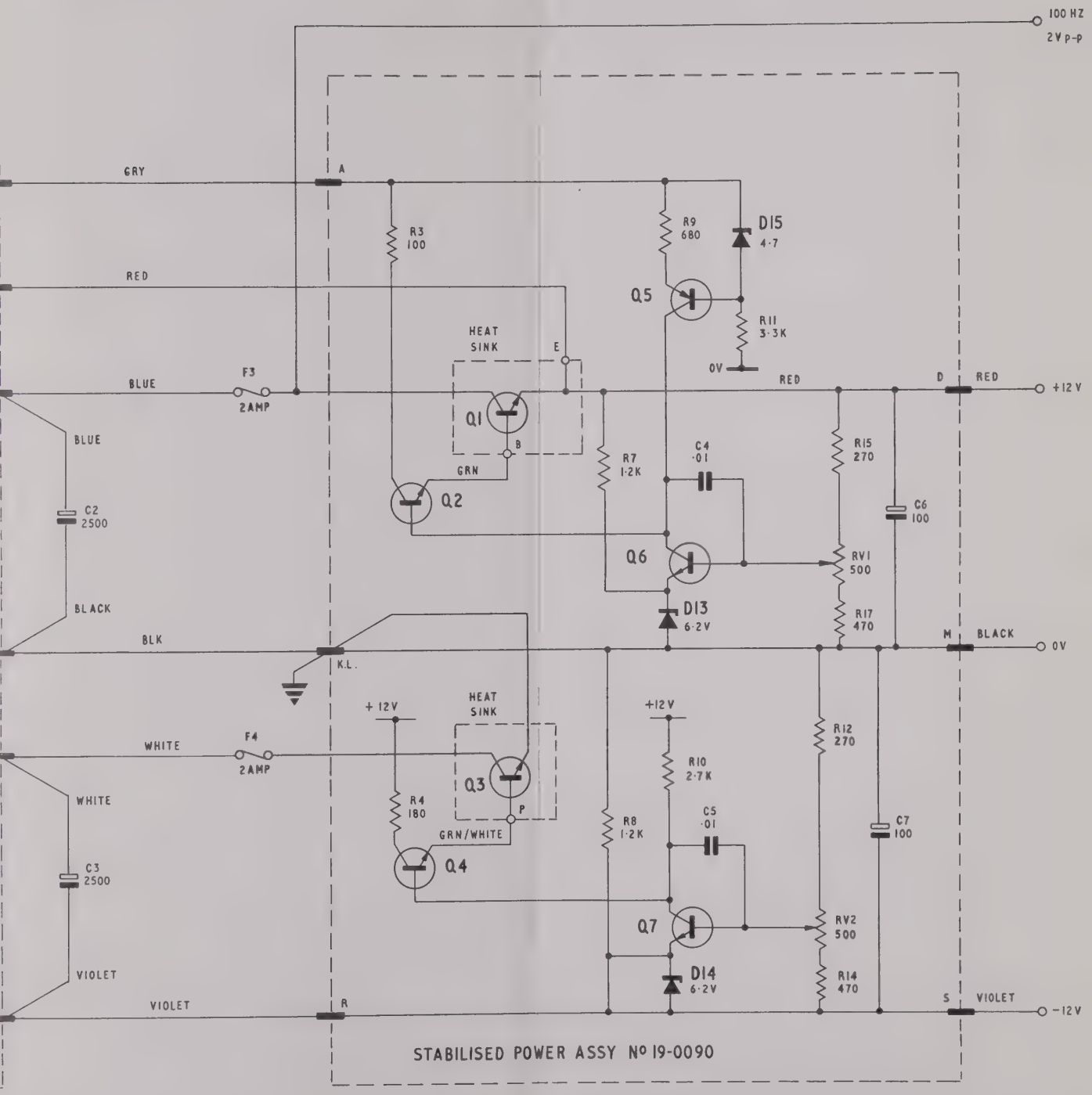
2. * THE VALUE SHOWN FOR RESISTOR R7 IS A NOMINAL ONE.
   THIS COMPONENT IS SUBJECT TO SELECTION ON TEST—
   SEE PARTS LIST.

ISSUE	
2	17·10·67 C.N.10535

EXTERNAL STANDARD ASSY. | 19-0160 SHT. 2 OF 2

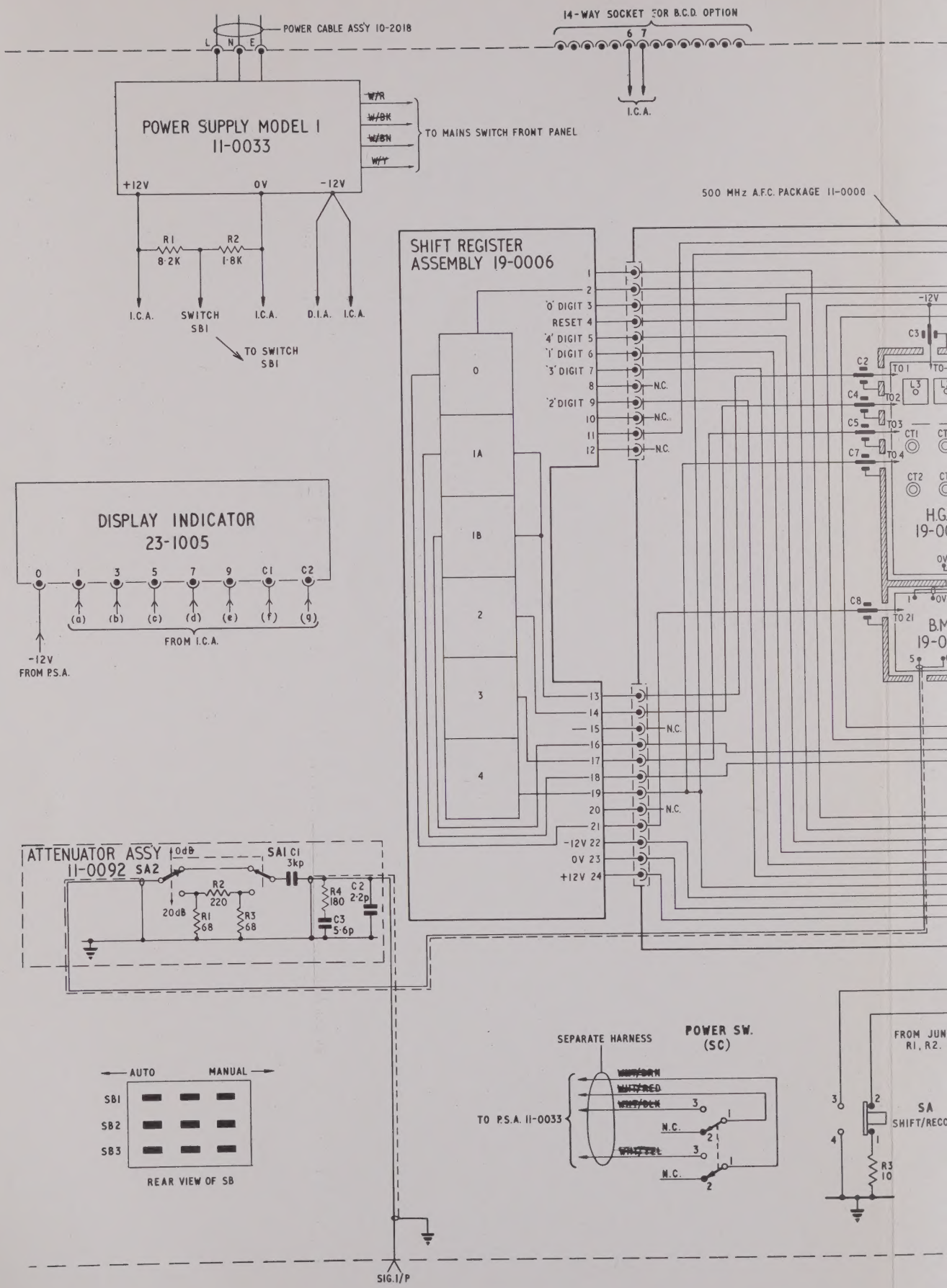


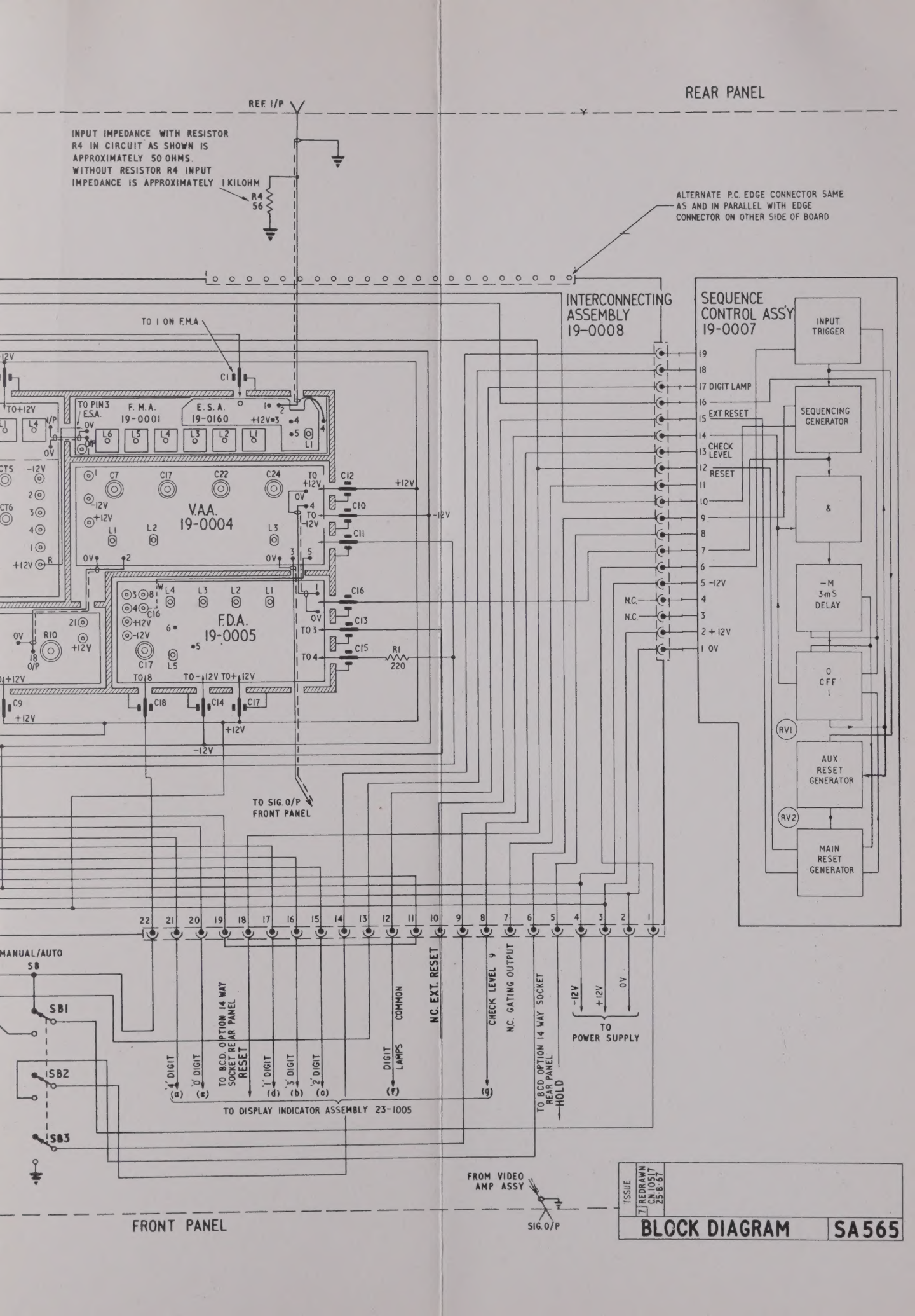
NOTE :
LINE AND NEUTRAL FUSES F1, F2
(a) FOR 240, 220, 200V OPERATION FIT 1 AMP FUSES
(b) FOR 120, 110V OPERATION FIT 2 AMP FUSES



ISSUE		
2	5·7·66	CN10234
3	5·12·66	CN10284
4	14·2·67	CN10343

CIRCUIT. POWER SUPPLY ASS'Y | 11-0033


POWER CABLE ASSY 10-2018
L N E
14-WAY SOCKET FOR B.C.D. OPTION
6 7
I.C.A.
POWER SUPPLY MODEL 1
11-0033
W/R
W/BK
W/BN
W/Y
TO MAINS SWITCH FRONT PANEL
+12V
0V
-12V
R1
8·2K
R2
1·8K
I.C.A.
SWITCH SB1
I.C.A.
D.I.A.
I.C.A.
TO SWITCH SB1
500 MHz A.F.C. PACKAGE 11-0000
SHIFT REGISTER ASSEMBLY 19-0006
0
1A
1B
2
3
4
1
2
'0' DIGIT 3
RESET 4
'4' DIGIT 5
'1' DIGIT 6
'3' DIGIT 7
8
'2' DIGIT 9
10
11
12
N.C.
N.C.
N.C.
13
14
15
16
17
18
19
20
21
-12V 22
0V 23
+12V 24
N.C.
N.C.
-12V
C3
C2
C4
C5
C7
C8
TO 1
TO 2
TO 3
TO 4
TO 21
L3
CT1
CT2
H.G.
19-0
B.M.
19-0
DISPLAY INDICATOR
23-1005
0
1
3
5
7
9
C1
C2
(a)
(b)
(c)
(d)
(e)
(f)
(g)
FROM I.C.A.
-12V
FROM P.S.A.
ATTENUATOR ASSY
11-0092 SA2
0dB
SA1 C1
3kp
20dB
R2
220
R1
68
R3
68
R4
180
C2
2·2p
C3
5·6p
AUTO
MANUAL
SB1
SB2
SB3
REAR VIEW OF SB
SEPARATE HARNESS
POWER SW.
(SC)
TO P.S.A. 11-0033
W/BRN
W/RED
W/BLK
N.C.
W/YEL
N.C.
FROM JUN
R1, R2.
SA
SHIFT/RECO
R3
10
SIG.I/P


REAR PANEL
REF I/P
INPUT IMPEDANCE WITH RESISTOR R4 IN CIRCUIT AS SHOWN IS APPROXIMATELY 50 OHMS. WITHOUT RESISTOR R4 INPUT IMPEDANCE IS APPROXIMATELY 1 KILOHM
R4 56
ALTERNATE P.C. EDGE CONNECTOR SAME AS AND IN PARALLEL WITH EDGE CONNECTOR ON OTHER SIDE OF BOARD
INTERCONNECTING ASSEMBLY 19-0008
SEQUENCE CONTROL ASS'Y 19-0007
INPUT TRIGGER
SEQUENCING GENERATOR
&
-M 3mS DELAY
O CFF I
AUX RESET GENERATOR
MAIN RESET GENERATOR
RV1
RV2
TO I ON F.M.A
TO PIN 3 E.S.A.
F.M.A. 19-0001
E.S.A. 19-0160
V.A.A. 19-0004
F.D.A. 19-0005
TO SIG. O/P FRONT PANEL
19 18 17 DIGIT LAMP 16 15 EXT RESET 14 13 CHECK LEVEL 12 RESET 11 10 9 8 7 6 5 -12V 4 N.C. 3 N.C. 2 +12V 1 0V
22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
MANUAL/AUTO SB
SB1
SB2
SB3
'1' DIGIT (a)
'0' DIGIT (e)
TO BCD OPTION 14 WAY SOCKET REAR PANEL
RESET
'1' DIGIT (d)
'3' DIGIT (b)
'2' DIGIT (c)
DIGIT LAMPS COMMON (f)
N.C. EXT. RESET
CHECK LEVEL 9 (g)
N.C. GATING OUTPUT
TO BCD OPTION 14 WAY SOCKET REAR PANEL
HOLD
-12V +12V 0V
TO POWER SUPPLY
TO DISPLAY INDICATOR ASSEMBLY 23-1005
FROM VIDEO AMP ASSY
SIG. O/P
FRONT PANEL
ISSUE 7 REDRAWN CN 10517 25-8-67
BLOCK DIAGRAM SA565

MP MASTER
MA24138